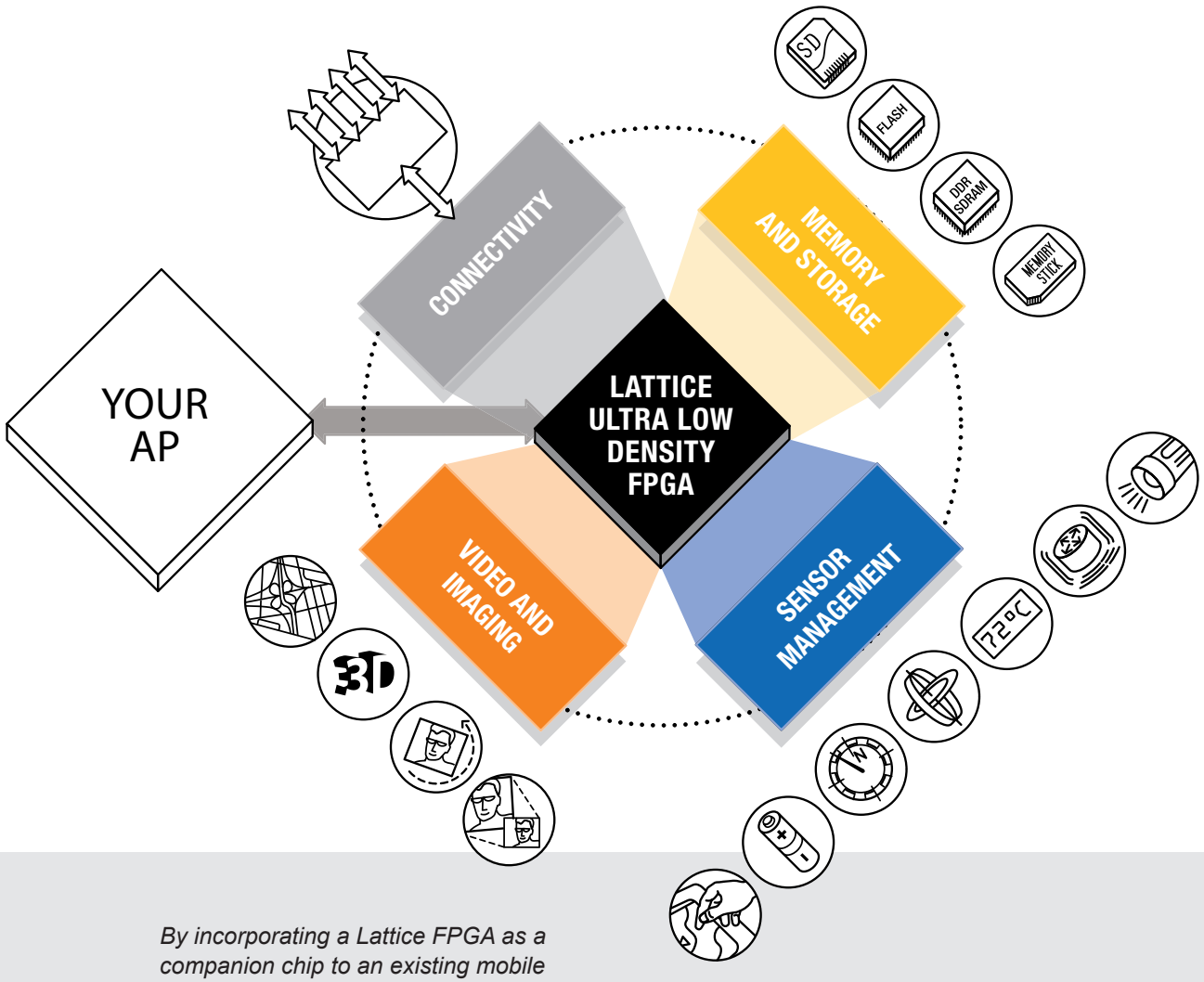
LATTICE SEMICONDUCTOR

Ultra Low Density FPGAs for Your Handheld Applications

LATTICESEMI.COM

Accelerate Your Handset



By incorporating a Lattice FPGA as a companion chip to an existing mobile chipset, mobile designers can quickly and easily evolve their platform with innovative features.

Mobile Handset Evolution

Mobile handsets are evolving at a tremendous rate, driven by changing use models, increasing competition, and emerging markets around the world. The average life of a handset is now much shorter than the development time required for mobile chipsets, throttling the ability for designers to add new generational hardware features. Today's mobile designers need a quick, easy way to meet their time to market requirements without compromising product innovation.

Ultra Low Density FPGAs

Ultra low density FPGAs from Lattice serve as a companion chip to existing Application Processors (APs), enabling handset designers to quickly and easily bring new features and capabilities to market. By utilizing FPGAs, mobile designers can ensure their product's competitive success.

Evolution with Lattice FPGAs

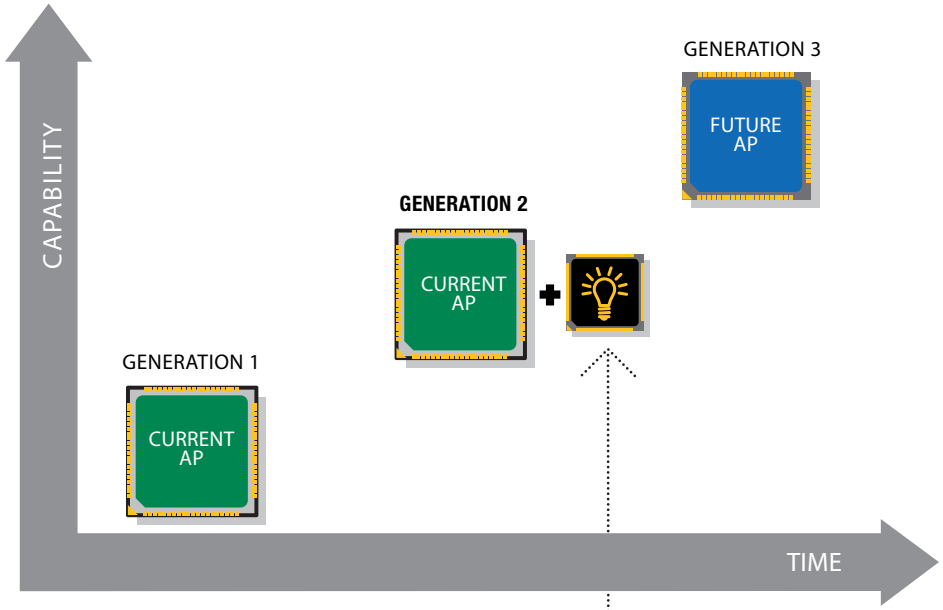
Your Idea, Just in Time

Application Processors are designed to support the most common features of today's mobile handsets. This means that a given application processor may not support the specific features designers need to differentiate their product. Furthermore, no processor will support any proprietary feature. How then does a mobile designer differentiate their platform from the competition?

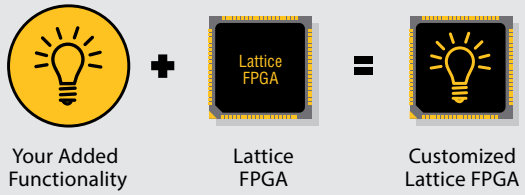
One choice may be to wait for the next generation of processors. Unfortunately, new application processors can take up to three years to define, design and manufacture. In addition, designers will still not be able to implement proprietary features.

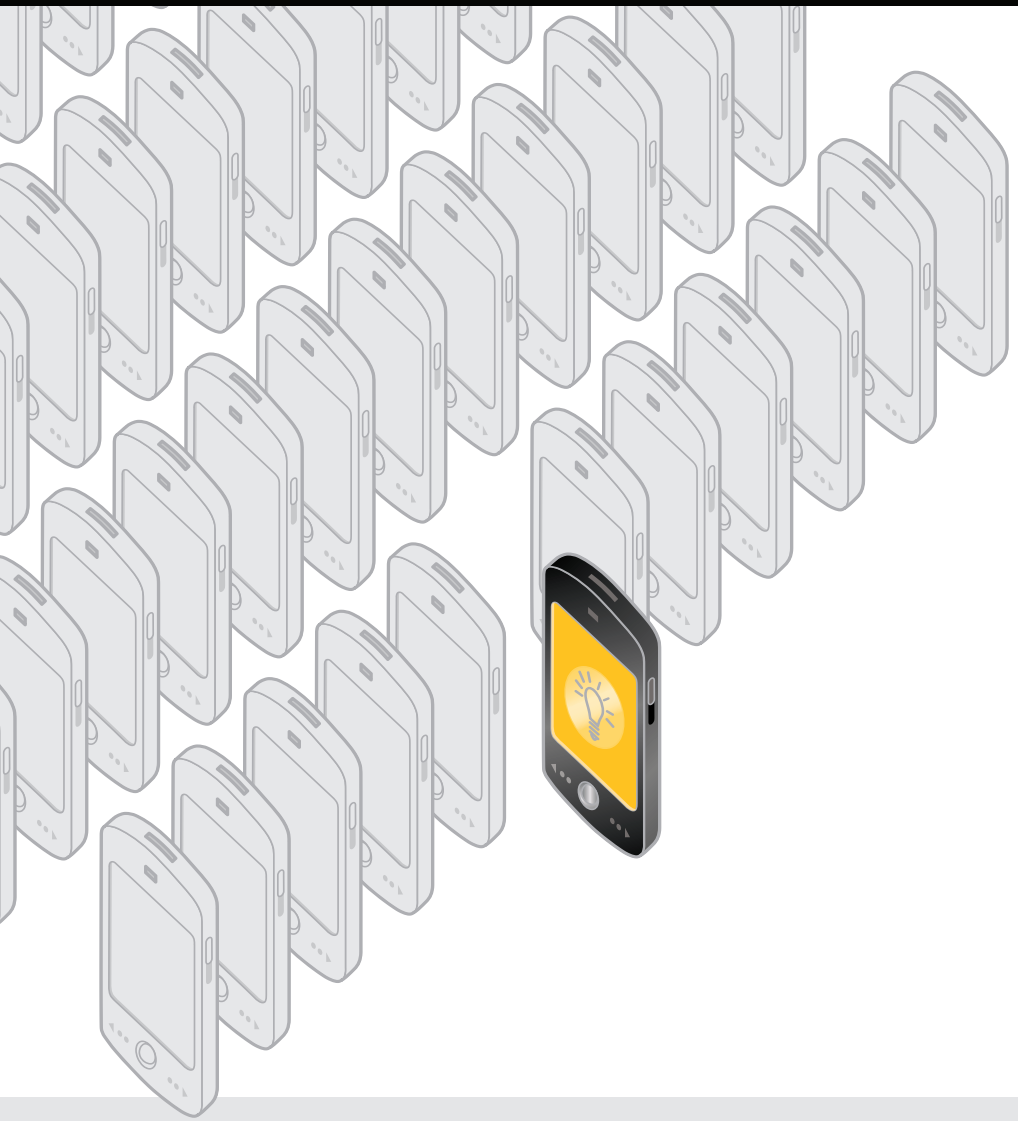
Companion to Application Processors

By using an FPGA as a companion to your existing application processor, you can bring new and differentiating features to market "off-cycle" from next generation mobile chipsets. Off-the-shelf Lattice FPGAs can be customized and in volume production within weeks.



Using a Lattice ultra low density FPGA as a companion to an existing Applications Processor allows new handsets with new and/or proprietary features to be developed without waiting for next-generation chipsets.



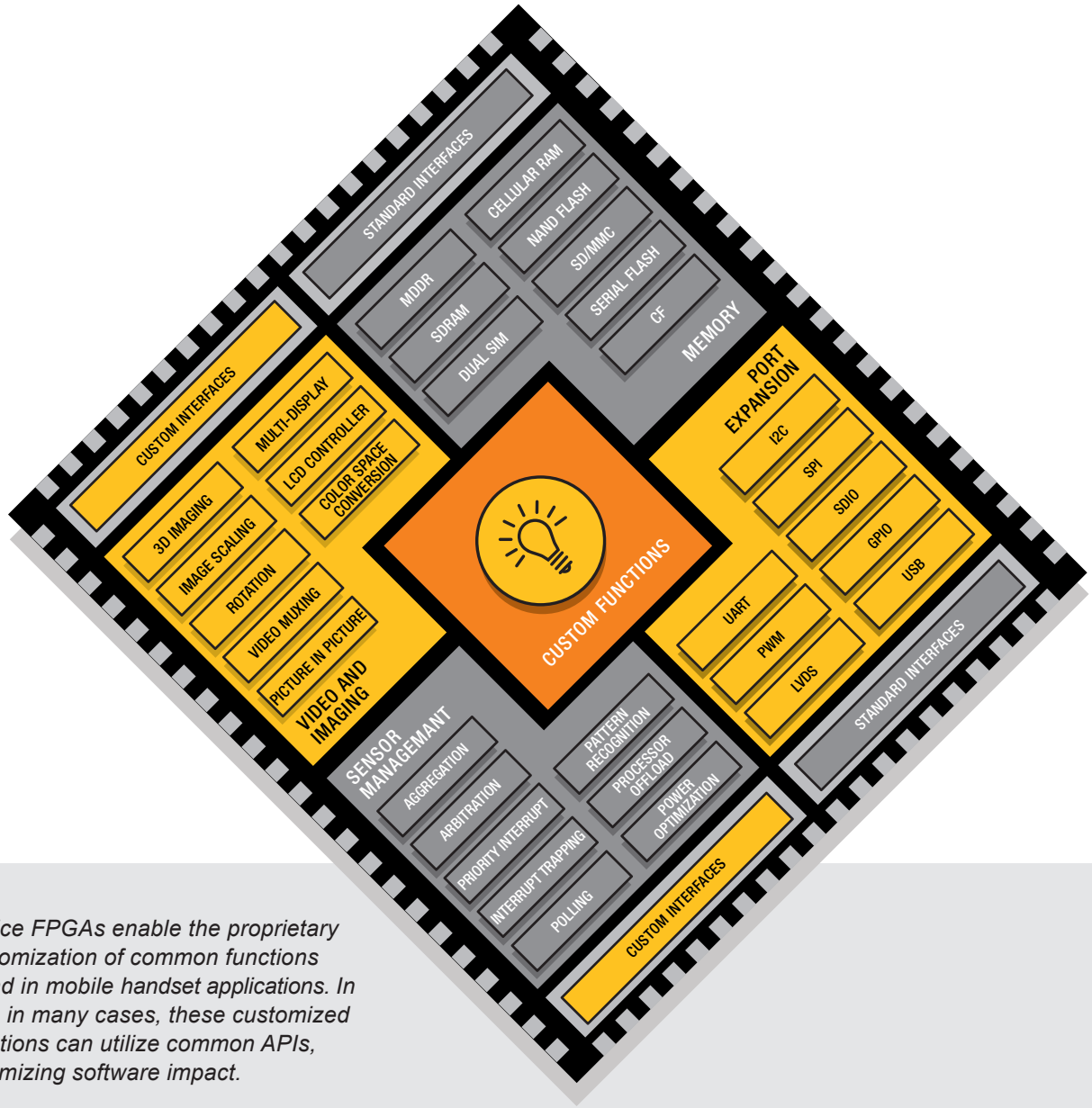


Lattice FPGAs Enable

Lattice ultra low density FPGAs allow designers to realize new and innovative features in their mobile handset. With an low cost, low power FPGA you can:

- Maximize product revenue by implementing proprietary, innovative ideas
- Preserve software investment by utilizing prior-generation mobile chipsets
- Lower costs by leveraging a common hardware platform across derivative products
- Avoid excessive software costs by utilizing standard APIs when adding sensors and peripherals
- Achieve on-time delivery by leveraging a flexible hardware platform to accelerate development

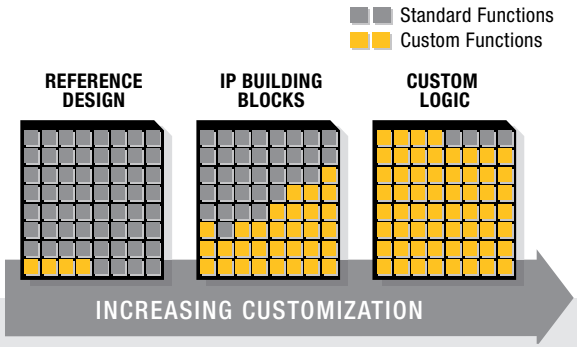
Differentiation



Lattice FPGAs enable the proprietary customization of common functions found in mobile handset applications. In fact, in many cases, these customized functions can utilize common APIs, minimizing software impact.

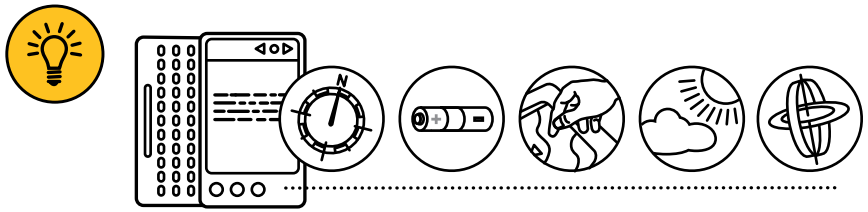
Lattice Design Services Can Help

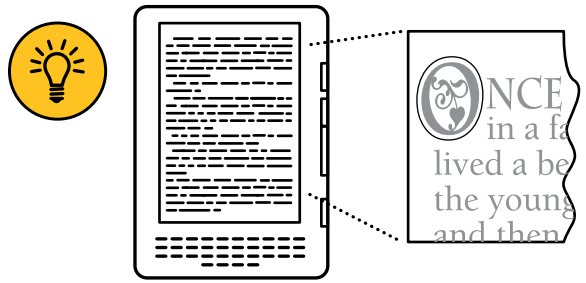
Lattice's design services team is available to help you take your idea to silicon. Every design has standard portions such as interfaces that may not change, as well as custom portions that differentiate your product and may be proprietary. To support the design process, Lattice can engage with you on different levels that include providing a complete reference design, providing tested and optimized IP building blocks, or delivering a full turn-key design. Lattice can even help you create the software drivers necessary to add new functionality to your system with ease.



Lattice can help you implement new features to your mobile application. Lattice can provide complete reference designs, IP building blocks, or even turn-key design services based on your design needs.

Customize your FPGA with Ease



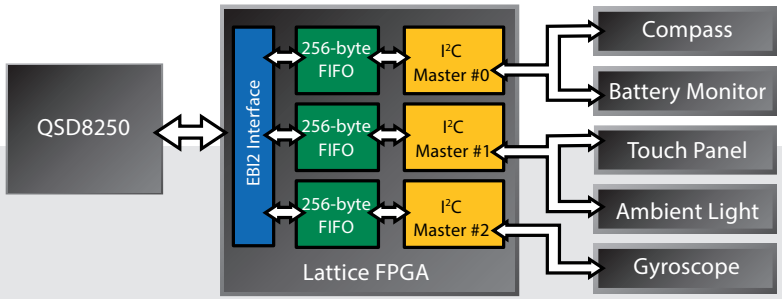


Sensor Expansion for Smartphone

Problem: A smartphone designer needed to add sensors to their existing platform. The problem was that their Applications Processor (AP) didn't have enough I²C ports to support the additional sensors.

Solution: Lattice worked with the customer to create an FPGA design that implemented additional I²C master controllers utilizing the AP's high bandwidth EBI2 bus.

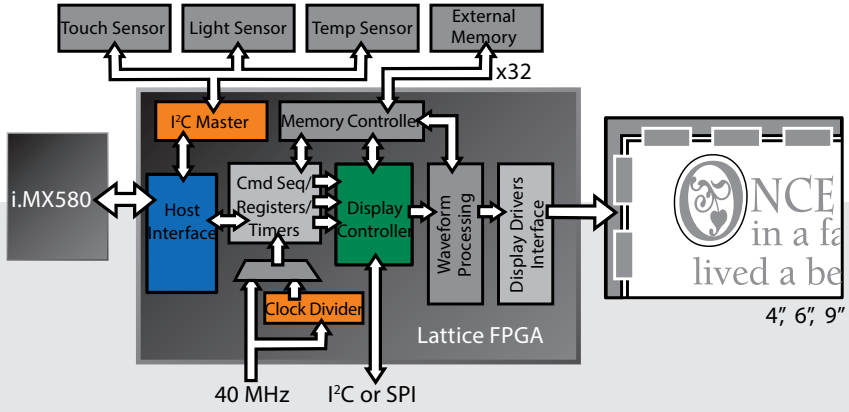
Three I²C master controllers operated independently and supported both 100 kHz (standard) and 400 kHZ (fast) operation modes, supporting standard and high performance sensors.

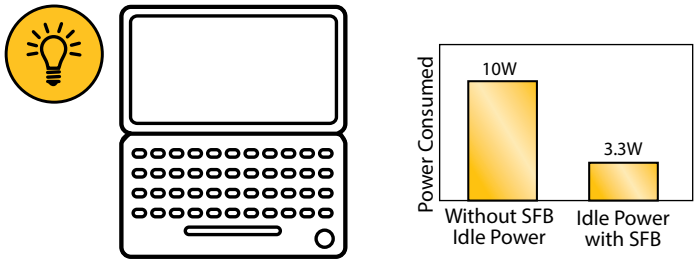


Display Controller for eBook Reader

Problem: An eBook reader manufacturer wanted to use an AP that didn't support the targeted electrophoretic display. In addition, a flexible display controller was needed to support different sized displays. Light and temperature sensors were also required to manage the quality of the display.

Solution: A Lattice FPGA was used to implement a display controller, I²C master for the sensors, a memory controller to external memory and an interface to their existing AP. Based on the sensors, display values were retrieved from external memory which determined how to drive the display. This design could be modified to support a 4", 6", or 9" display.

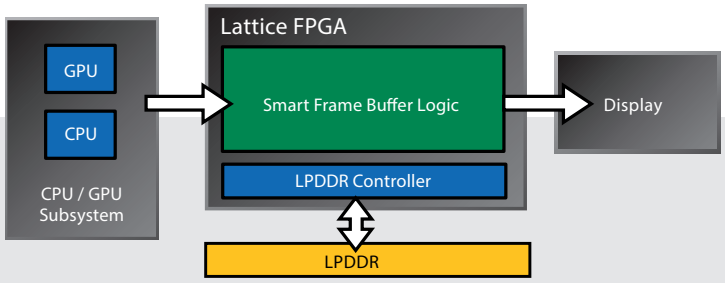


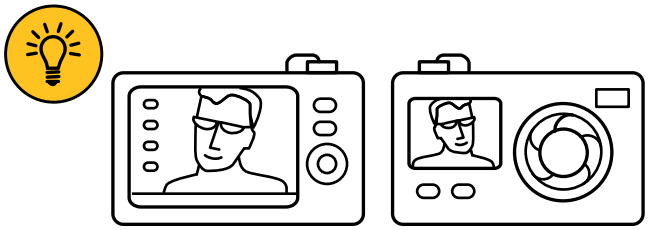


Smart Frame Buffer for Ultrabooks and Notebooks

Problem: A manufacturer of Ultrabooks wanted to reduce power consumption and increase battery life while still delivering the same performance of the display subsystem. The manufacturer needed a companion chip to manage the outputs of the GPU and CPU while reducing total system power.

Solution: The Lattice Smart Frame Buffer solution enables Ultrabook / Notebook suppliers to increase battery life by shutting down the GPU and or CPU subsystems during periods of inactivity. The smart frame buffer manages and refreshes the display while the power hungry CPU/GPU subsystem goes into standby.

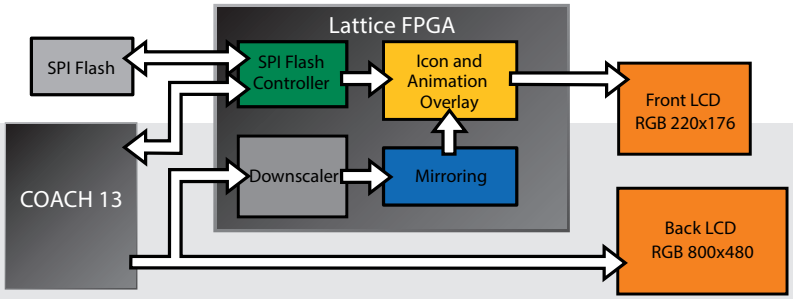




Dual Display for Digital Still Camera

Problem: A manufacturer of a new type of Digital Still Camera wanted to add a front display. The manufacturer also wanted to support different images and animation on the front screen. The problem was that the customer's AP only supported a single display.

Solution: Lattice worked with the customer to implement functionality to support the front display using a Lattice FPGA. A downscaler was implemented to convert the resolution of the image going to the back display to the resolution of the front display. In addition, text-over-graphic and animation capabilities were also implemented, reading data from the SPI flash memory.



Ultra Low Density FPGAs

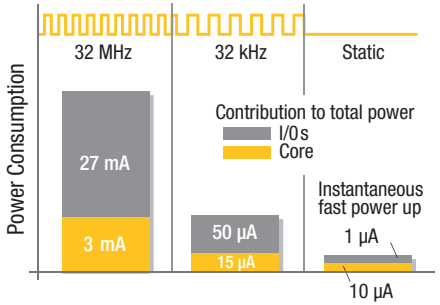
Ultra-low power

Maximum battery life is always an objective for mobile handheld applications. Lattice ultra-low power FPGAs have been optimized to achieve low power at any speed.

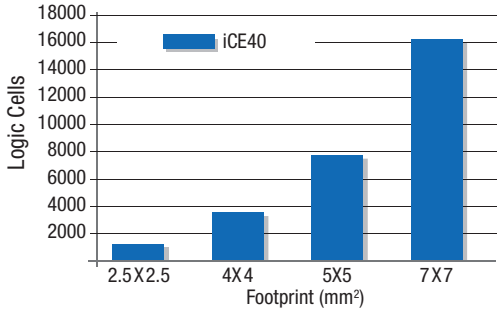
Designed for mobile applications

Mobile applications have a very limited bill of materials budget. With this in mind, iCE40™ devices are designed to be extremely cost effective. First, to achieve ASIC-like costs, the number of I/Os for every family member has been carefully chosen. In addition, since iCE40 FPGA devices are manufactured using a 40-nm process geometry, they offer the industry's highest logic capacity per I/O, and the lowest cost per logic cell.

Traditional semiconductor products cannot meet the flexibility and time-to-market requirements needed in today's mobile applications. With Lattice's ultra low density FPGAs, mobile handheld designers now have a flexible option that meets the necessary ultra-low power, small footprint, and low cost requirements needed for today's fast-paced mobile development.

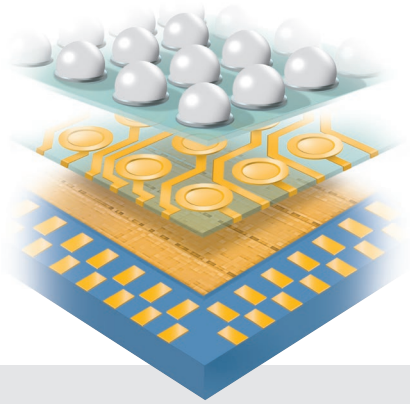


With Lattice's ultra low density FPGA portfolio, designers can achieve standby currents as low as 10 µA, extending battery life for mobile applications.



Industry's most advanced packages

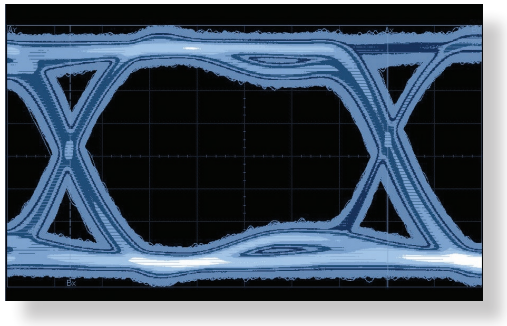
Lattice ultra low density FPGAs use the most advanced packaging technology available to meet the aggressive requirements of mobile, portable and extremely space-constrained devices. Lattice's iCE40 FPGAs are available in packages as small as 2.5 x 2.5mm, allowing designers to quickly integrate more functionality into a significantly smaller space.



Wafer Level Chip Scale Packaging enables standard mounting balls to be attached directly to the die via a redirection layer, minimizing board space and device costs.

Optimized for video applications

Ultra low density FPGAs from Lattice have been optimized to support video applications. With on-chip memory, a phase-locked loop, and differential I/O, Lattice FPGAs can support video transmit bandwidths up to 758 Mbps, supporting a variety of video display resolutions.



The MachXO2 family can drive and receive LVDS video supporting up to 756 Mbps.

ASIC-like solution enables a seamless prototype-to-production development flow

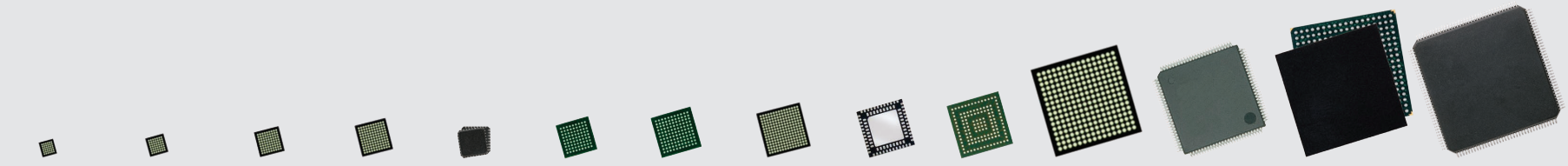
The SRAM-based fabric of the iCE40 devices can be configured during prototyping using external SPI FLASH or a download cable.

In production, the embedded Non-Volatile Configuration Memory (NVCM) can be programmed with your design, eliminating the need for external memory while securing your design against external interrogation. Custom markings are available.

iCE40: Lowest Cost, Smallest Footprint, Lowest Power

	LP-Series Optimized for ultra-low power applications (1.0 Volt and 1.2 Volt Operation)				HX-Series Optimized for display, memory and SERDES applications (1.2 Volt Operation)		
Feature	**LP384**	**LP1K**	**LP4K**	**LP8K**	**HX1K**	**HX4K**	**HX8K**
Logic Cells	384	1280	3520	7680	1280	3520	7680
Embedded RAM Bits	0	64K	80K	128K	64K	80K	128K
Phase-Locked Loops	0	1	2	2	1	2	2
Core Icc @ 0KHz[1]	21µA	100µA	360µA	360µA	267µA	667µA	1100µA
Package	**Programmable I/O: Max I/O (LVDS Channels)**						
32-pin QFN (5 x 5 mm)	21 (4)						
36-ball ucBGA (2.5 x 2.5 mm)	25 (3)	25 (3)[2]					
49-ball ucBGA (3 x 3 mm)	37 (6)	35 (5)					
81-ball ucBGA (4 x 4 mm)	55 (3)	63 (8)	63 (9)[2]				
81-ball csBGA (5 x 5 mm)		62 (8)					
84-pin QFNS[2] (7 x 7 mm)		67 (7)					
100-pin TQFP/VQFP (14 x 14 mm)					72 (9)[2]		
121-ball ucBGA (5 x 5 mm)		95 (12)	93 (13)	93 (13)			
121-ball csBGA (6 x 6 mm)		92 (12)					
132-ball csBGA (8 x 8 mm)					95 (11)	95 (12)	95 (12)
144-pin TQFP (20 x 20 mm)					96 (12)	107 (14)	
225-ball ucBGA (7 x 7 mm)			167 (20)	178 (23)			178 (23)
256-ball caBGA (14 x 14 mm)							206 (26)

1. At 1.2V Vcc
2. No PLL Available
3. Only 1 PLL Available

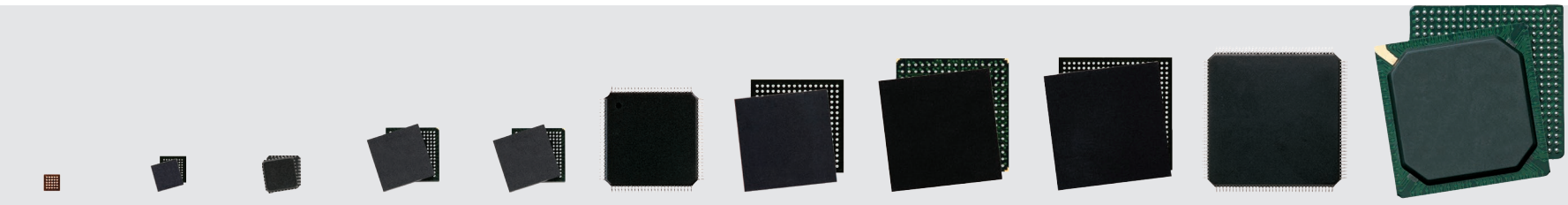


36 ucBGA	49 ucBGA	81 ucBGA	121 ucBGA	32 QFN	81 csBGA	121 csBGA	225 ucBGA	84 QFNS	132 csBGA	256 caBGA	100 TQFP/VQFP	FT324	144 TQFP
.4 mm pitch	.4 mm pitch	.4 mm pitch	.4 mm pitch	.5 mm pitch	.5 mm pitch	.5 mm pitch	.4 mm pitch	.5 mm pitch	.5 mm pitch	.8 mm pitch	.5 mm pitch	1.0 mm pitch	.5 mm pitch
2.5 X 2.5 mm	3 X 3 mm	4 X 4 mm	5 X 5 mm	5 X 5 mm	5 X 5 mm	6 X 6 mm	7 X 7 mm	7 X 7 mm	8 X 8 mm	14 X 14 mm	14 X 14 mm	19 X 19 mm	20 X 20 mm

MachXO2: Best I/O and Embedded Functionality

	ZE, HC, and HE-Series								
Feature	**XO2-256**	**XO2-640**	**XO2-640U[1]**	**XO2-1200**	**XO2-1200U[1]**	**XO2-2000**	**XO2-2000U[1]**	**XO2-4000**	**XO2-7000**
LUTs	256	640	640	1280	1280	2112	2112	4320	6864
EBR RAM (Kbits)	0	18	64	64	74	74	92	92	240
EBR RAM Blocks (9 Kbits/Block)	0	2	7	7	8	8	10	10	26
Distributed SRAM (Kbits)	2	5	5	10	10	16	16	34	54
User Flash Memory (Kbits)	0	24	64	64	80	80	96	96	256
PLLs	0	0	1	1	1	1	2	2	2
Package & I/O Combinations									
25-ball WLCSP[2] (2.5 x 2.5 mm)				18					
32-pin QFN (5 x 5 mm)	21								
64-ball ucBGA (4 x 4 mm)	44								
100-pin TQFP (14 x 14 mm)	55	78		79		79			
132-ball csBGA (8 x 8 mm)	55	79		104		104		104	
144-pin TQFP (20 x 20 mm)			107	107		111		114	114
184-ball csBGA[3] (8 x 8 mm)								150	
256-ball caBGA (14 x 14 mm)						206		206	206
256-ball ftBGA (17 x 17 mm)					206	206		206	206
332-ball caBGA (17 x 17 mm)								274	278
484-ball fpBGA (23 x 23 mm)							278	278	334
Typical Static Power									
ZE (mW)	0.019	0.033		0.070		0.098		0.153	0.230
HC (mW)	4	7	13	13	18	18	32	32	48
HE (mW)						2	3	3	5

1. Ultra high I/O count devices are supported for HC/HE options.
2. WLCSP packages are offered for ZE devices only.
3. Contact your Lattice sales representative regarding this package, available for HE option only.

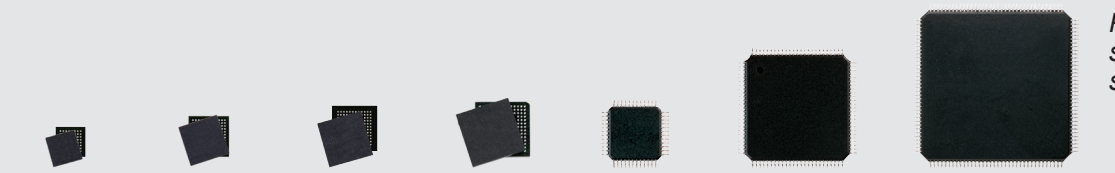


Packages are shown actual size.

25 WLSCP	64 ucBGA	32 QFN	132 csBGA	184 csBGA	100 TQFP	256 caBGA	256 ftBGA	332 caBGA	144 TQFP	484 fpBGA
.4 mm pitch	.4 mm pitch	.5 mm pitch	.5 mm pitch	.5 mm pitch	.5 mm pitch	.8 mm pitch	1.0 mm pitch	.8 mm pitch	.5 mm pitch	1.0 mm pitch
2.5 X 2.5 mm	4 X 4 mm	5 x 5 mm	8 X 8 mm	8 X 8 mm	14 X 14 mm	14 X 14 mm	17 X 17 mm	17 X 17 mm	20 x 20 mm	23 X 23 mm

ispMACH 4000ZE: Low Cost, Low Power CPLD

	ZE-Series			
Features	**4032ZE**	**4064ZE**	**4128ZE**	**4256ZE**
Macrocells	32	64	128	256
t_{PD} (ns)	4.4	4.7	5.8	5.8
t_{CO} (ns)	3.0	3.2	3.8	3.8
t_S (ns)	2.2	2.5	2.9	2.9
f_{MAX} (MHz)	260	241	200	200
V_{CC} (Volts)	1.8	1.8	1.8	1.8
Typical Standby Current (µA)	10	11	12	13
Package	**I/Os + Inputs**			
48-pin TQFP (7 x 7 mm, 0.5 mm pitch)	32 + 4	32 + 4		
64-ball csBGA (5 x 5 mm, 0.5 mm pitch)	32 + 4	48 + 4		
64-ball ucBGA (4 x 4 mm, 0.4 mm pitch)		48 + 4		
100-pin TQFP (14 x 14 mm, 0.5mm pitch)		64 + 10	64 + 10	64 + 10
132-ball ucBGA (6 x 6 mm, 0.4 mm pitch)			96 + 4	
144-ball csBGA (7 x 7 mm, 0.5 mm pitch)		64 + 10	96 + 4	108 + 14
144-pin TQFP (20 x 20 mm, 0.5mm pitch)			96 + 4	96 + 4



64 ucBGA .4 mm pitch 4 X 4 mm | 64 csBGA .5 mm pitch 5 X 5 mm | 132 ucBGA .4 mm pitch 6 X 6 mm | 144 csBGA .5 mm pitch 7 x 7 mm | 48 TQFP .5 mm pitch 7 X 7 mm | 100 TQFP .5 mm pitch 14 X 14 mm | 144 TQFP .5 mm pitch 20 X 20 mm

Packages are shown actual size.

Development Tools

Mobile Design Efficiency

Design cycles for today's mobile applications are becoming shorter than ever before. Customer demand and stiff competition are forcing designers to bring products with new features to market constrained by tight development schedules. Design cycles that once took more than 2 years to complete have now shortened to 6 months or less. Thus, design efficiency is more important than ever before.

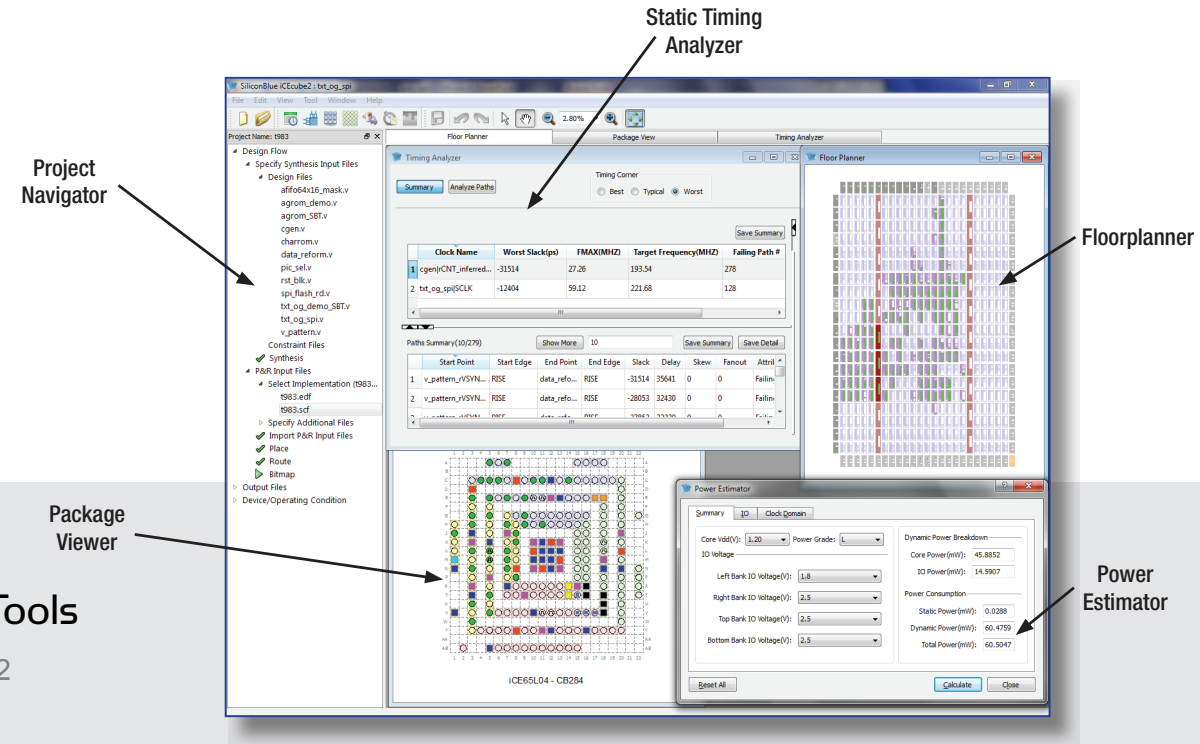
Lattice offers an integrated development system for the mobile designer. Lattice's iCEcube2™ development system, Diamond design software, and easy-to-use development kits deliver world class set of tools for improving design efficiency.

Comprehensive iCEcube2 Development Tools for iCE40 and iCE65 Devices

iCEcube2™ supports standard HDL-based design flow incorporating industry-leading Synplify Pro® synthesis tools from Synopsys®. iCEcube2 support both Microsoft® Windows® and Red Hat® Linux® operating systems.

Lattice Diamond Design Software for MachXO2 Devices

Lattice Diamond design software offers leading-edge design and implementation tools optimized for cost sensitive, low-power Lattice FPGA architectures. Diamond features design exploration, ease of use, improved design flow, and numerous other enhanced features.



iCEcube2 Development System Design Environment

More Information on Lattice Development Tools

iCEcube2 Development Tools: www.latticesemi.com/iCEcube2

Diamond Development Tools: www.latticesemi.com/diamond

Consumer Applications Intellectual Property

Optimized Solutions

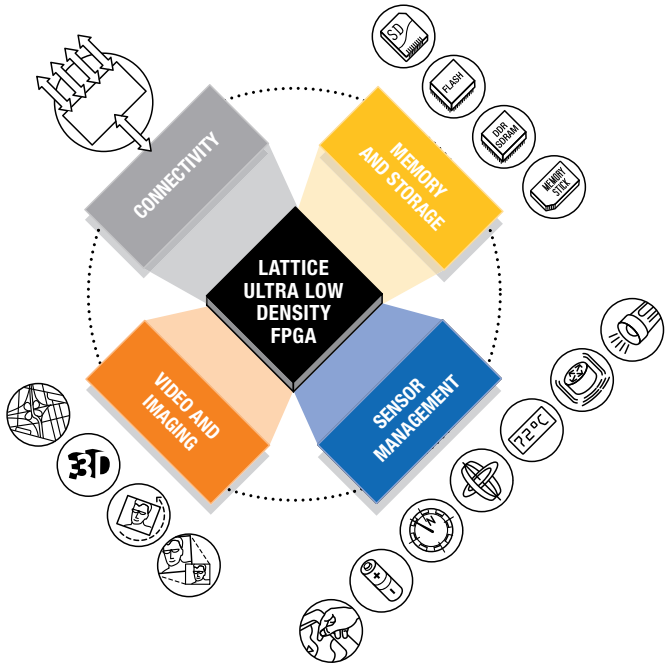
Lattice offers a wide range of intellectual property geared towards consumer applications to help accelerate your design innovation. These proven IP Cores are optimized for Lattice's ultra low density FPGA architectures targeting consumer applications.

CONNECTIVITY
1-to-4 UART Expander
CMOS Camera Interface
PWM (16x3)
I²C Master / Slave Controller
SPI Master / Slave Controller
USB 2.0 Host Controller
USB 2.0 Device Controller
USB 2.0 OTG Controller
USB 2.0 Hub Controller
I²C Master / Slave Controller
PCI Master / Target Controller

SENSOR MANAGEMENT
I²C Master Controller
SPI Master Controller
SLIMbus Client Controller
UART
Expansion Memory Interface
Touchscreen Controller
PWM (16x3)
Keypad Scanner
IrDA Fast Tx/Rx

VIDEO AND IMAGING
Dual Display Controller
Graphics LCD Controller
LCD Controller (16x2 Character)
Touch Screen Controller
XGA to WVGA LANCZOS2 Scaler
XGA to WVGA Nearest Neighborhood Scaler
RGB565 to YCbCr 8bit (Color Space Conversion)
RGB666 to YCbCr 8bit (Color Space Conversion)
RGB888 to YCbCr 8bit (Color Space Conversion)
YCbCr 10bit to RGB666 (Color Space Conversion)
YCbCr 10bit to RGB888 (Color Space Conversion)
YCbCr 10bit to RGB565 (Color Space Conversion)
YCbCr 8bit to RGB565 (Color Space Conversion)
YCbCr 8bit to RGB888 (Color Space Conversion)
YCbCr 8bit to RGB666 (Color Space Conversion)
I²C Based Video Switching
Image Blending – Multiple Images and Text Overlay
Image Enhancements – Brightness and Contrast Controller
LVDS Transmitter/Receiver
LVDS Serializer/De-Serializer
DVI Receiver Controller
MIPI DSI Receiver / Transmitter Controller
MIPI CSI-2 Receiver / Transmitter Controller
Dual-LVDS Transmitter (after LVDS Serializer)

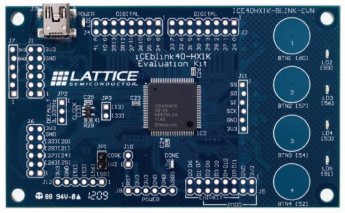
OTHER
Sigma-Delta ADC
Mico8 Microcontroller
LED/OLED Driver
Power Management Bus Controller
CRC (Cyclic Redundancy Checker)
AES Encryption / Decryption
RC4-based pseudo-random sequence generator
MIPI Battery Interface (BIF)



MEMORY AND STORAGE
Cellular RAM Controller
MDDR Controller
CF+Controller
MS Pro Interface
NAND Flash Interface
SLC2MLC Interface
MMC Host Controller
SD Host Controller
SDIO Host Controller
MMC Client – MMC Mode Using FPGA RAMs as Memory
SD Client – SD Mode Using NAND Flash as Memory
NOR Flash Controller
Flash Controller with Wear Leveling
LPC Bus Controller
DDR/DDR2/LPDDR Memory Controllers
SDRAM Controller

Development Kits

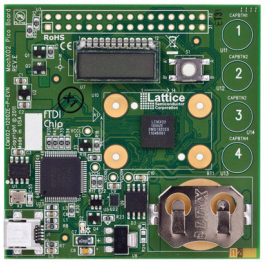
iCEblink40 Evaluation Kit



Features

- Two versions:
  - High Performance: iCE40HX1K-VQ100
  - Low Power: iCE40LP1K-QN84
- Powered by USB input
- 1Mbit SPI PROM (enough for two iCE40HX1K images using WarmBoot)
- Four capacitive-touch buttons (requires FPGA logic)
- Four user LEDs
- Dual PMOD header compatible with Digilent PMOD boards (6x2 header)
- 3.33 MHz oscillator (can be modified to support 33.33 MHz or 333 kHz)
- 1.2V and 3.3V power supplies
- All iCE40HX1K I/O available on headers or 0.1" through-holes

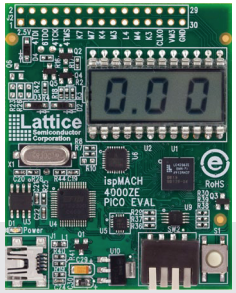
MachXO2 Pico Development Kit



Features

- MachXO2 LCMXO2-1200ZE
- 4-character 16-segment LCD display
- 4 capacitive touch sense buttons
- 1 Mbit SPI Flash
- I²C temperature sensor
- Current and voltage sensor circuits
- Expansion header for JTAG, I²C
- Standard USB cable for device programming and I²C communication
- RS-232/USB & JTAG/USB interface

ispMACH 4000ZE Pico Development Kit



Features

- Pre-programmed Pico Power Demo
- ispMACH 4000ZE device (LC4256ZE-5MN144C)
- Power Manager II device (ispPAC-POWR6AT6-01SN32I)
- LCD panel
- USB mini jack socket for power, JTAG programming, and I²C interface
- 2X15 header landing for off-board expansion provides access to LC4256ZE GPIOs, POWR6AT6 VMON inputs, I²C, and JTAG chain

MachXO2 and ispMACH 4000ZE Breakout Board Evaluation Kits

Features

- Preprogrammed with hardware test program
- LEDs
- Expansion Header Landings
- Prototyping Area
- USB Mini Jack Socket (Program/Power)
- JTAG Header Landing
- RoHS-compliant packaging and process
- USB connector cable

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Additionally, customers can receive technical support for Lattice's Programmable Logic Products from our Asia based applications group, by contacting Lattice Asia applications during the hours of 8:30 a.m. to 5:30 p.m. Beijing Time (CST) +0800 UTC (Chinese and English language only).
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March 2013
Order #: I0225C