THE GROWING USE OF PROGRAMMABLE LOGIC DEVICES IN MOBILE HANDSETS

A Lattice Semiconductor White Paper

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Introduction

The pace of innovation in the mobile handset industry has never been higher, with users continuing to demand more from these devices. Smart phones, tablets and other battery-powered devices have evolved beyond communication devices and now offer personal assistance by unifying "always connected" features such as navigation, email, phone, Internet access and camera. Choosing between the two leading smartphone operating systems, smartphone designers depend on their physical hardware to differentiate their products and position them against competitive products. This is an area where programmable logic devices add direct value by providing mobile handset system architects a way to quickly innovate and add new functionality to their products. Below are some examples of why and how low cost, low power programmable logic devices are successfully adding value to mobile handset design.

Asynchronous Product Development Cycles within the Handset Industry

Readers of this white paper may not be surprised to learn that the product design life cycles of mobile handset and chipset vendors are fundamentally different. It is fairly common to see new phone models being introduced every other month, while chipset vendors release newer versions of their chipsets in a much slower product cycle cadence. While there are solid and obvious reasons for this, the challenge faced by handheld system architects is also real; i.e. keeping up with product innovation cycles that are faster than what the chipset vendors are capable of supporting. A good example of this is the recent announcement of the MIPI battery interface (BIF) standard.

The MIPI Battery Interface (BIF) Standard

The use of dual-core and quad-core processors, along with the marketing imperative to create a compelling user experience, increases power consumption that has direct downstream effects on power delivery, battery life and longevity. Striking a balance

among optimal power delivery, battery capacity, chemistry, safety and form factor is a significant design challenge. The communication protocol established by MIPI-BIF provides a method for system designers to read parameters on demand to optimize power consumption during device use and to optimize battery charging. It also provides a method to authenticate batteries for systems that need to ensure user safety. Although the MIPI standard has already been announced, chipset vendors will still need time to adopt this standard in their products. However, handset designers may want to take advantage of MIPI-BIF much sooner. Programmable logic devices are perfectly suited in such situations, because they enable mobile system architects to adopt new standards using existing chipset or application processors. In fact, soon after MIPI released the BIF standard, Lattice Semiconductor announced its support for the standard and that it is engaged with key customers on implementing it.

Figure 1 illustrates the use of a low cost, low power FPGA to create a bridge between an existing application processor and the recently released MIPI-BIF standard. Communication over the BIF battery communication line (BCL) is enabled using the low power FPGA. On the application processor side, I^2C, because it is commonly available, is a natural choice to connect the host application processor to the FPGA. A simple protocol is defined on top of the I^2C standard to communicate between the host and the FPGA. If needed, the host interface can be easily customized using the FPGA solution. In addition, further customization of the BIF interface / protocol can also be achieved when using an FPGA. Furthermore, the FPGA offers the flexibility for customers to even integrate other functions within the same low power FPGA device. By using a low power FPGA as a companion chip to the application processor, handset manufacturers can enable cutting edge features / standards into their products on demand to create clear product differentiation.
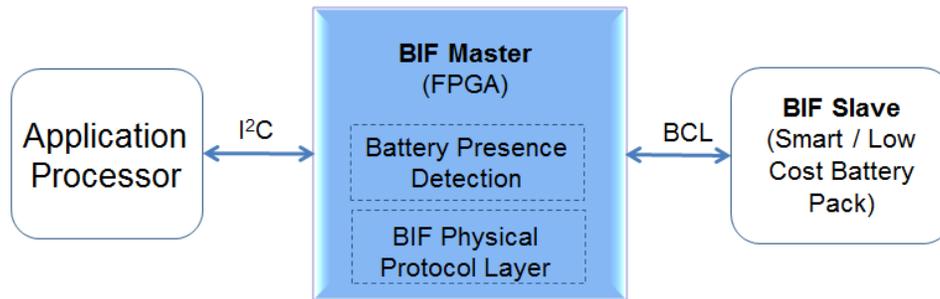
Figure 1 - Using a Low Power FPGA to Implement New Standards

Loss of Flexibility Due To Unsupported Standards by Chipset Vendors

Although system-on-a-chip and holistic integration are the mantras of most chipset manufacturers, chipsets are often designed to meet broad market needs and therefore may not support certain standards. This denies handset system architects valuable flexibility. Also, as new standards are adopted by chipset manufacturers, they often completely drop older ones from their portfolio. This again takes away valuable flexibility from both the system architect and the component procurement teams of handset manufacturers. Often in such cases, system architects may want to use the latest chipset solutions based on their merits, while the procurement team may wish to continue using certain older standards, even if not supported by the latest chipsets, to provide supply flexibility. Here again FPGAs provide considerable value.

Figure 2 illustrates how a low cost, low power FPGA can be used to regain design flexibility by providing an easy way to bridge between two different standards. Figure 2 shows how a terrestrial TV broadcast tuner chip with a custom interface can be used with an applications processor that does not support that interface. Figure 2 shows the host interface through the SPI bus that is commonly available in application processors. Here again, communication to the application processor can be customized as needed when using a FPGA.
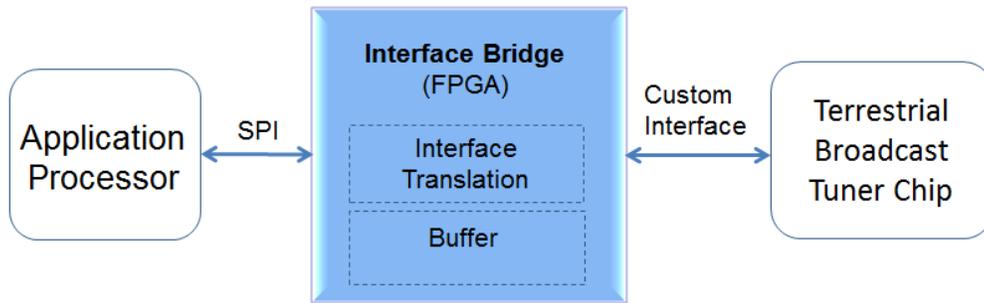
Figure 2 - Low power FPGA Used as an Interface Bridge

Sensor Management

The number of sensors included in smartphones has grown dramatically. High-end smartphones include several sensors like gyroscope, multiple cameras, touch, accelerometers, magnetometers, ambient light sensor and GPS, among others. In the future, phones are expected to be even more aware of their surroundings (sensing altitude, temperature, humidity, etc.) while providing more value-added features such as the monitoring of human vital signs. The proliferation of sensors has a profound impact on the user experience. For example, most smartphone users can confirm that the use of GPS navigation has a direct and noticeable impact on battery life. In addition, some smartphone operating systems mandate the frequency of polling from certain critical sensors, such as touch. Touch sensors may need to be polled at frequencies of several hundred KHz to ensure a compelling user experience. In architectures where the application processors are connected to sensors directly, sensors need to be actively managed by the application processors, which have a direct impact on power consumption.

Figure 3 illustrates an implementation of a low power FPGA used as a companion chip to the application processor to manage sensors in a mobile platform. Independent I^2C masters may be used to manage different sensors to ensure the right throughput is achieved from each sensor. Sensors, such as touch, that require higher throughput may be interfaced to the FPGA using an independent I^2C bus, if required. The smart sensor hub may be designed with intelligence to aggregate interrupts generated from

different sensors and, based on pre-defined conditions, to interrupt the application processor. This design approach would enable the application processor to go into a standby state for longer periods of time and thereby reduce power consumption, or would free the application processor to perform other important tasks.
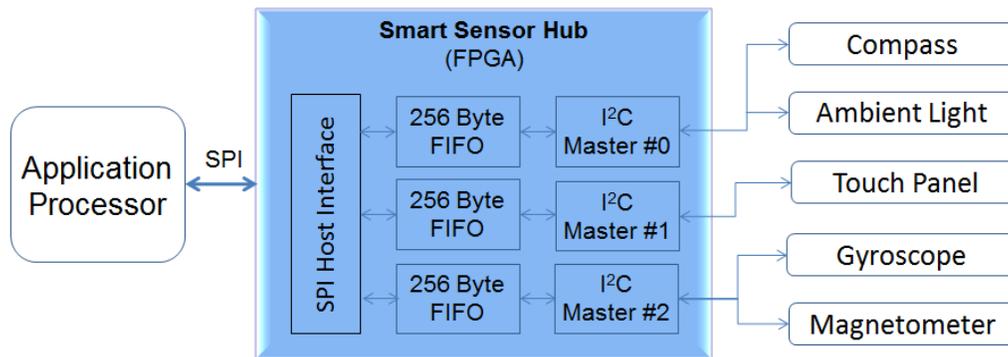

Figure 3 - Using an FPGA as a Smart Sensor Hub

Conclusion

The mobile handset market is extremely competitive, with many handset models offered by multiple manufacturers. The product development cadence of handset manufacturers is different from those of chipsets or application processors. In some cases, this creates a bottleneck for handset manufacturers to enable cutting edge features in their products on demand. In addition, product differentiation has become a key challenge that is magnified because handsets using the same operating system appear to deliver a similar user experience to consumers. Therefore, handset manufacturers use hardware features to differentiate their products. Handset system architects are constantly trying to strike a balance among new feature inclusion, reducing power consumption and keeping cost in check. In such a dynamic environment, low cost, low power FPGAs, such as the iCE40 devices offered by Lattice Semiconductor, are a perfect choice to help handset architects design new features to differentiate their products.

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