Minimize Cost and Power, Maximize Value

Industry Leading Ultra Low Density FPGA Portfolio

Lattice provides the most complete and comprehensive portfolio of ultra low density FPGAs - suitable for applications ranging from instant-on system control, flexible I/O expansion, to those that require ultra low cost and low power with optimized features for glue logic and bridging. From mobile handsets to leading-edge telecommunications infrastructure, Lattice offers a solution that minimizes cost and power while maximizing value. Two great complementary families to solve the range of system level issues that are faced by designers.

iCE40: Lowest Cost, Smallest Footprint, Lowest Power

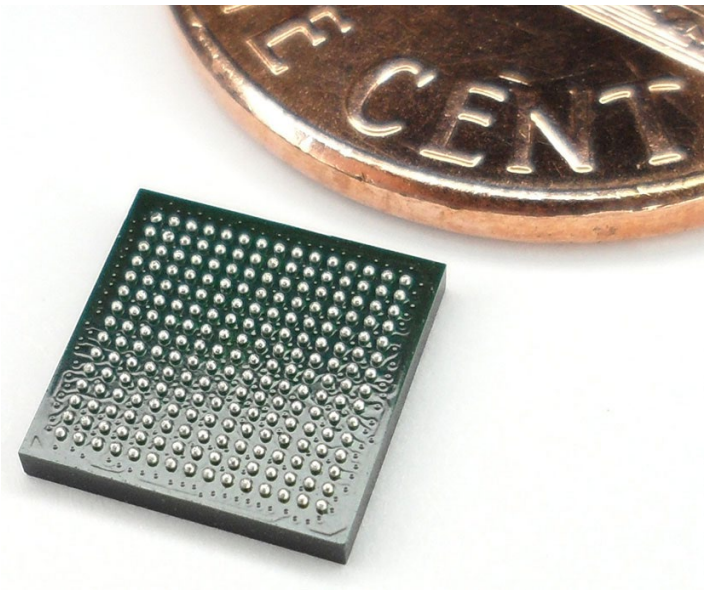
The iCE40™ family of FPGAs is designed for applications that have the most aggressive power, cost and footprint requirements. Ideally architected for smartphones, tablets, digital still cameras, and other space and power constrained systems, the iCE40 family uses a highly cost optimized fabric. This family is a popular choice for functions such as sensor management, video and imaging, custom connectivity, memory / storage expansion and glue logic.

iCE40 FPGAs are available in two series: low power (LP) and high performance (HX).

MachXO2: Best I/O and Embedded Functionality

The MachXO2™ family of non-volatile, single chip reprogrammable FPGAs is optimized for applications that require the highest number of feature rich I/O for I/O expansion applications. Plus, with an on-chip regulator, embedded Flash and hard IP, MachXO2 devices are ideally suited for instant-on multi-voltage system control functionality. Combining an optimized SRAM based look-up table (LUT) architecture together with embedded Flash technology, the affordable MachXO2 family is the industry's most feature rich, ultra low density FPGAs for cost-sensitive system designs.

MachXO2 FPGAs are available in three options: high performance (HC, HE) and low power (ZE).



Two Families Providing the Most Benefits in the Ultra Low Density FPGA Segment

- **Affordability**
  - Optimized for a wide variety of cost sensitive applications
- **Ultra-Low Power**
  - Power as low as 25µA static
- **Feature Rich**
  - Instant-on, power up in less than 1ms
  - Pre-engineered source synchronous I/O supports DDR, DDRX2, DDRX4
  - Optimized for HD quality video – MIPI-DBI/DPI
- **Broad Package Portfolio with Choices of Ultra Small Footprint and Highest I/O**
  - Footprints as small as 2.5 x 2.5 mm
  - Up to 334 I/O
  - 0.4 mm BGA pitch suited for smartphones and tablet applications

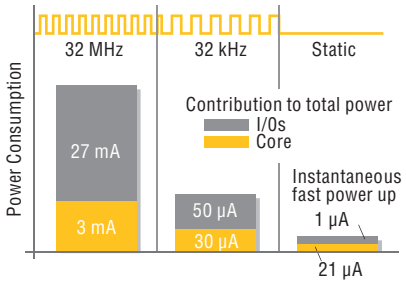
iCE40: Best Value, Smallest Footprint, Lowest Power

Overview

iCE40 FPGAs offer the industry's most affordable ultra low density FPGA. Using a 40nm process with unique non-volatile configuration memory, The iCE40 family is optimized for cost sensitive applications including smartphones, digital cameras, tablets and any other applications requiring cost sensitive glue logic and bridging. With standby currents as low as 10µA, iCE40 FPGAs enable designers of power constrained devices to quickly and easily bring new features and capabilities to market. Available in the world's smallest plastic 0.4mm pitch BGA packages, the iCE40 family offers significant savings in board space.

Ultra-low power

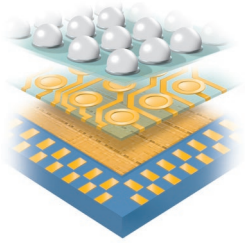
Maximum battery life is critical for mobile handheld applications. Lattice iCE40 FPGAs have been optimized to achieve low power at any speed.



With Lattice's iCE40 FPGAs, designers can achieve standby currents as low as 21µA, extending battery life for mobile applications.

Advanced Small Form Factors

iCE40 FPGAs use the most advanced packaging technology available to meet the aggressive requirements of mobile, portable and extremely space-constrained devices. iCE40 FPGAs are available in packages as small as 2.5 x 2.5mm, allowing designers to quickly integrate more functionality into a significantly smaller space.



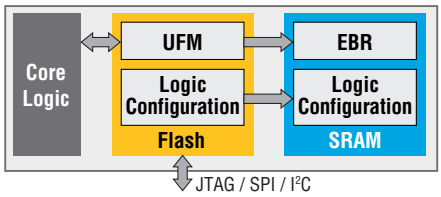
MachXO2: Best I/O and Embedded Functionality

Overview

MachXO2 FPGAs are designed to offer an unprecedented mix of low cost and high functionality in a single device. Through the use of 65nm embedded Flash technology and innovative design, MachXO2 devices deliver high system performance, a robust architecture, support for enhanced I/O features, on-chip User Flash Memory, on-chip regulator, hardened control functions and flexible security features.

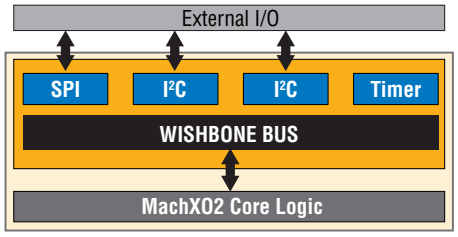
On-chip Flash Memory

- **Storage for both user data and device logic configuration**
- **Non-volatile, instant-on (less than 1ms) and in a single device – all while maintaining reprogrammability**



Embedded Function Blocks

- **Hard implementations of two I²C and one SPI interface cores, and a timer/ counter**
- **All functions are accessible both externally and within the device**

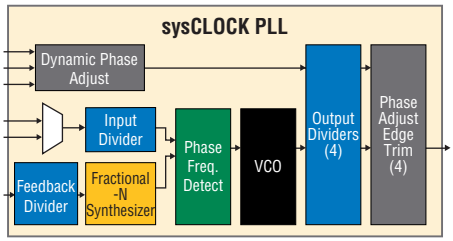


sysIO™ Buffers

- **Programmable sysIO supports a wide range of interfaces**
  - LVTTL, LVCMOS (3.3/2.5/1.8/1.5/1.2)
  - PCI, LVDS, Bus-LVDS, MLVDS
  - RSDS, LVPECL
  - SSTL 25/18, HSTL 18
- **Input hysteresis, hot socketing and on-chip differential termination**

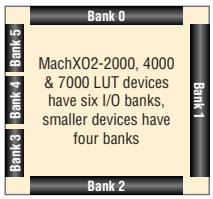
Advanced Clocking Technology

- **Full featured PLL**
- **On-chip oscillator with +/-5% accuracy and 2-133MHz operation**



Asymmetrical I/O Banking

- **Each device has asymmetrical I/O banks to flexibly connect to different interfaces**
- **Supports 1.2, 2.5 or 3.3V core voltages**



Two Great Low Density FPGA Choices

			iCE40	MachXO2
Feature	**Ultra Low Cost**	Optimized architecture to support cost sensitive applications	✓	–
	Small Form Factor Packages	Package offering below 10mm²	4	1
	Vcc Supply Voltage	MachXO2 offers available on-chip voltage regulator	1.2V	1.2, 2.5, 3.3V
	External Configuration	Configure at power-up from external source	SPI, µP	JTAG, SPI, µP
	Non-volatile Configuration	On-chip configuration memory	Non-volatile Configuration Memory (1 cycle)	Embedded Flash (10K programming cycles)
	Instant-on Configuration Time	Power-up time in milliseconds	<25ms	<1ms
	Hardened I²C and SPI	Minimizes the use of LUTs for implementing additional functionality	–	✓
	High I/O Density	Triple staggered I/O increases total I/O count. Asymmetrical banking scheme maximizes I/O usage. Low cost BGA packages reduce cost per I/O.	–	✓

iCE40 Application Examples

Smart Sensor Hub using iCE40

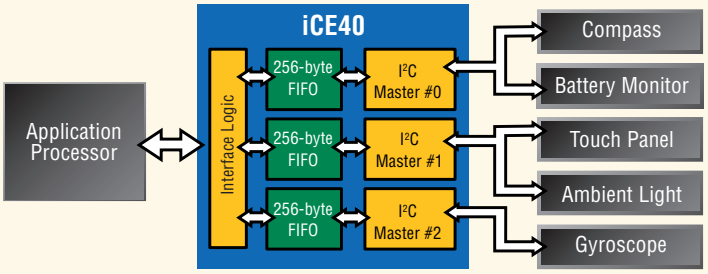
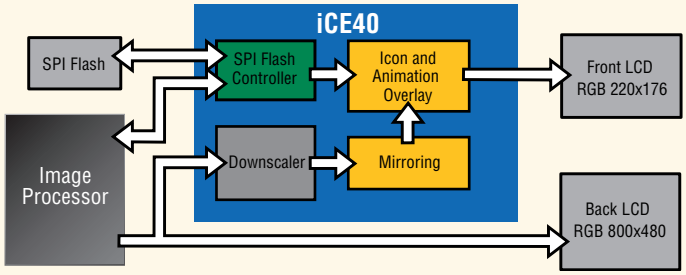
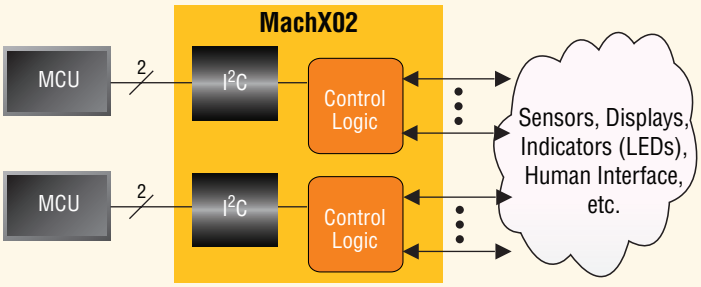


Image Management using iCE40

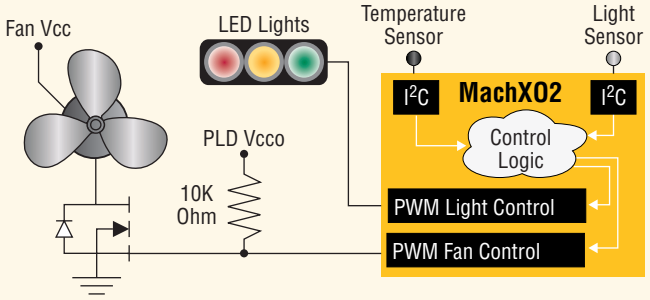


MachXO2 Application Examples

High Performance I/O Expansion using MachXO2

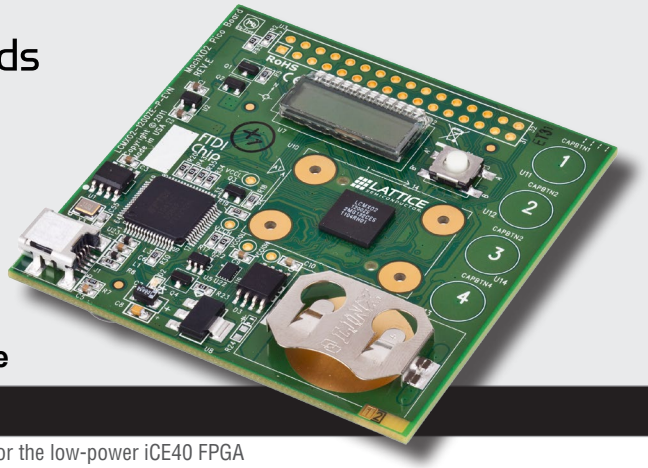


System Control using MachXO2



Development Kits and Evaluation Boards

Lattice offers a number of development kits and evaluation boards that provide a complete and easy-to-use platform to evaluate the performance of the iCE40 and MachXO2 families, or aid in the development of custom designs. For more information on development hardware and tools, go to www.latticesemi.com/products/developmenthardware.



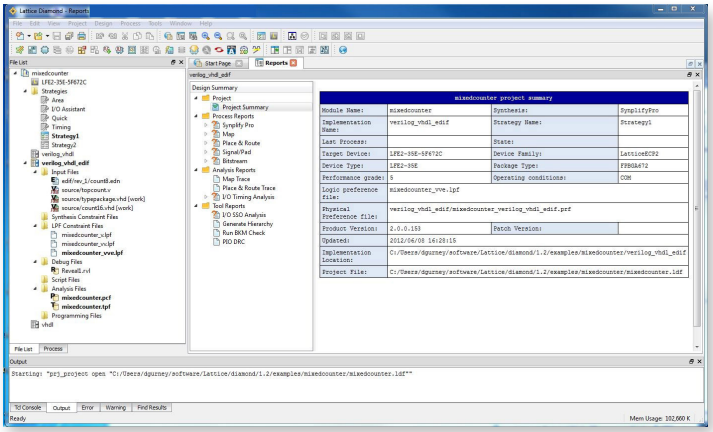
Development Kit and Evaluation Board Selection Guide

Product	Device	Description
iCEblink40™ Evaluation Kit	iCE40LP1K, iCE40HX1K	Low-cost platform for the low-power iCE40 FPGA • Easy USB for programming, debugging, virtual I/O functions and power • Four capacitive-touch buttons & LEDs • 1Mbit SPI serial configuration PROM
iCEman40™ Evaluation Kit	iCE40HX8K	Easy-to-use platform for rapidly prototyping iCE40 FPGAs • USB programming, debugging, virtual I/O functions, and power supply • Four user LEDs, 27.0 MHz and 32.768 kHz clock sources • Five differential input pairs and five differential output pairs
MachXO2 Pico Development Kit	XO2-1200ZE	Low-cost development platform for MachXO2 • Battery or USB power; USB I/O and programming • 4-character LCD display plus 4 capacitive touch sense buttons and I²C temperature sensor • Power measurement via delta sigma A2D conversion
MachXO2 Breakout Board	XO2-1200ZE	Simple low-cost board that provides complete I/O access to the MachXO2 • LEDs, Prototyping Area • Power and Program via USB • Downloadable demos
MachXO2 Control Development Kit	XO2-4000HC	Full featured MachXO2 development platform for system control • XO2-4000HC FPGA with 4320 LUTs • Up to two 7:1 LVDS sources and one output • 128Mbit LPDDR memory and 4Mbit SPI Flash • Current and voltage sensor circuits, MicroSD memory card socket, expansion headers

Design Tools for iCE40 and MachXO2

Lattice provides complete leading-edge design and implementation tools optimized for cost sensitive, low-power Lattice FPGA architectures such as: iCE40 and MachXO2 FPGAs. MachXO2 devices are supported by Lattice Diamond® design software, and iCE40 is supported by iCEcube2™ design software. Comprehensive design flows enable users to quickly perform design entry, IP configuration, simulation, implementation, timing analysis, power analysis and device programming.

The development tools integrate Synopsys' Synplify Pro® synthesis tool and also include the Aldec Active-HDL™ simulation solution, with an RTL/gate-level mixed-language simulator. In addition to Synplify Pro for all devices, Lattice Diamond offers Lattice Synthesis Engine (LSE) for MachXO2 devices to provide additional synthesis exploration options.



Lattice development software offers superior design exploration tools

Device Selection Guide

	iCE40							MachXO2					
Feature	**LP384**	**LP1K**	**LP4K**	**LP8K**	**HX1K**	**HX4K**	**HX8K**	**256**	**640/U**	**1200/U**	**2000/U**	**4000**	**7000**
Logic Cells	384	1280	3520	7680	1280	3520	7680	256	640	1280	2112	4320	6864
Embedded RAM Bits	0	64K	80K	128K	64K	80K	128K	0	18K/64K	64K/74K	74K/92K	92K	240K
Phase-Locked Loops	0	1	2	2	1	2	2	0	0/1	1	1/2	2	2
Core Icc @ 0KHz[1]	21µA	100µA	360µA	360µA	267µA	667µA	1100µA	18µA	28µA	56µA	80µA	124µA	189µA
Memory Standards	LPDDR							DDR / DDR2 / LPDDR					
LVDS Speed	525Mbps							756Mbps					
Package	**Programmable I/O: Max I/O (LVDS Channels)**												
25-ball WLCSP (2.5 x 2.5 mm)[5]										18			
32-pin QFN (5 x 5 mm)	21 (4)							21					
36-ball ucBGA (2.5 x 2.5 mm)	25 (3)	25 (3)[2]											
49-ball ucBGA (3 x 3 mm)	37 (6)	35 (5)											
64-ball ucBGA (4 x 4 mm)								44					
81-ball ucBGA (4 x 4 mm)	55 (3)	63 (8)	63 (9)[3]										
81-ball csBGA (5 x 5 mm)		62 (8)											
84-pin QFNS[2] (7 x 7 mm)		67 (7)											
100-pin TQFP/VQFP (14 x 14 mm)					72 (9)[2]			55	78	79	79		
121-ball ucBGA (5 x 5 mm)		95 (12)	93 (13)	93 (13)									
121-ball csBGA (6 x 6 mm)		92 (12)											
132-ball csBGA (8 x 8 mm)					95 (11)	95 (12)	95 (12)	55	79	104	104	104	
144-pin TQFP (20 x 20 mm)					96 (12)	107 (14)			107[4]	107	111	114	114
184-ball csBGA (8 x 8 mm)[6]												150	
225-ball ucBGA (7 x 7 mm)			167 (20)	178 (23)			178 (23)						
256-ball caBGA (14 x 14 mm)							206 (26)				206	206	206
256-ball ftBGA (17 x 17 mm)										206[4]	206	206	206
332-ball caBGA (17 x 17 mm)												274	278
484-ball fpBGA (23 x 23 mm)											278[4]	278	334

1. MachXO2 (ZE option) measured at 1.2V Vcc
2. No PLL available in this package
3. Only 1 PLL available
4. Ultra high I/O count devices are supported for XO2-HC/HE options
5. WLCSP package available for ZE option only
6. Contact Lattice sales representative regarding this package, available for HE option only

Applications Support
techsupport@latticesemi.com

July 2013
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