RGB565 to YCbCr 8-Bit Converter

April 2013 Reference Design RD1154

Introduction

RGB565 to 8-bit YCbCr converter converts RGB color space to YCbCr 4:2:2 color space. To facilitate easy insertion to practical video systems, this design example takes video stream control signals (H_SYNC, V_SYNC, and DEN) and delays them appropriately, so that control signals can be easily synchronized with the output video stream. This document provides a brief description of RGB565 to YcbCr 8-bit Converter and its implementation.

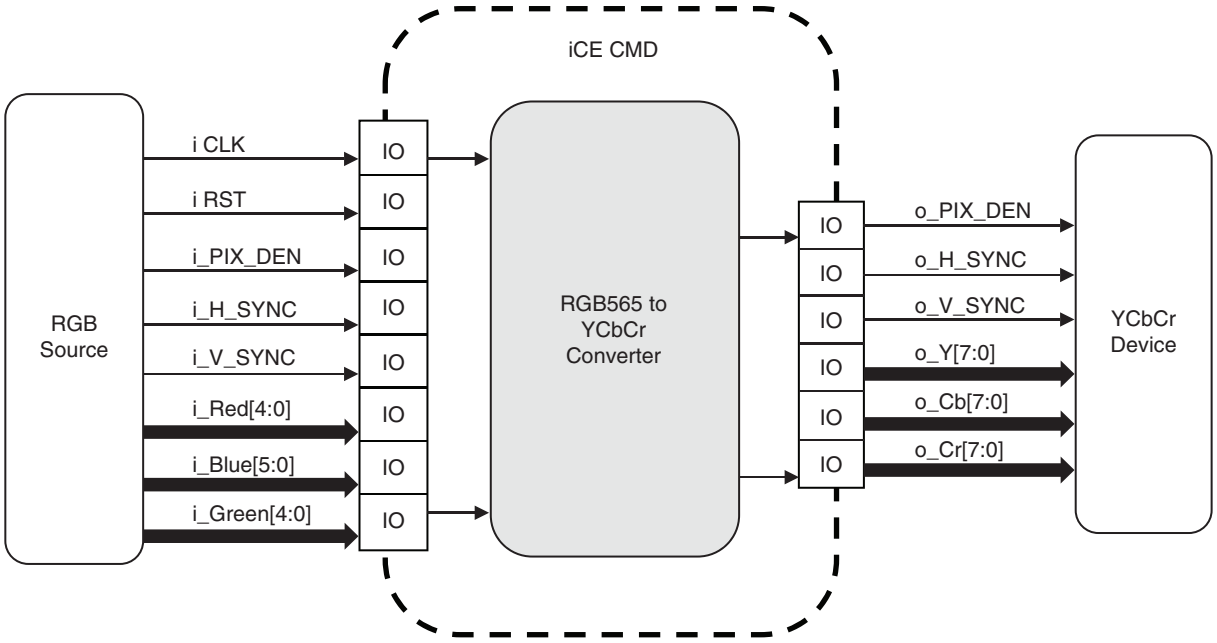
The design is implemented in VHDL. The Lattice iCEcube2™ Place and Route tool integrated with the Synopsys Synplify Pro® synthesis tool is used for the implementation of the design. The design can be targeted to other iCE40™ FPGA product family devices.

Features

- RGB565 mode input and 8-bit YCbCr 4:2:2 mode output
- Pipelined implementation
- Latency of 5 cycles
- H_SYNC, V_SYNC and DEN control signals for video synchronization

Functional Description

Figure 1. Functional Description



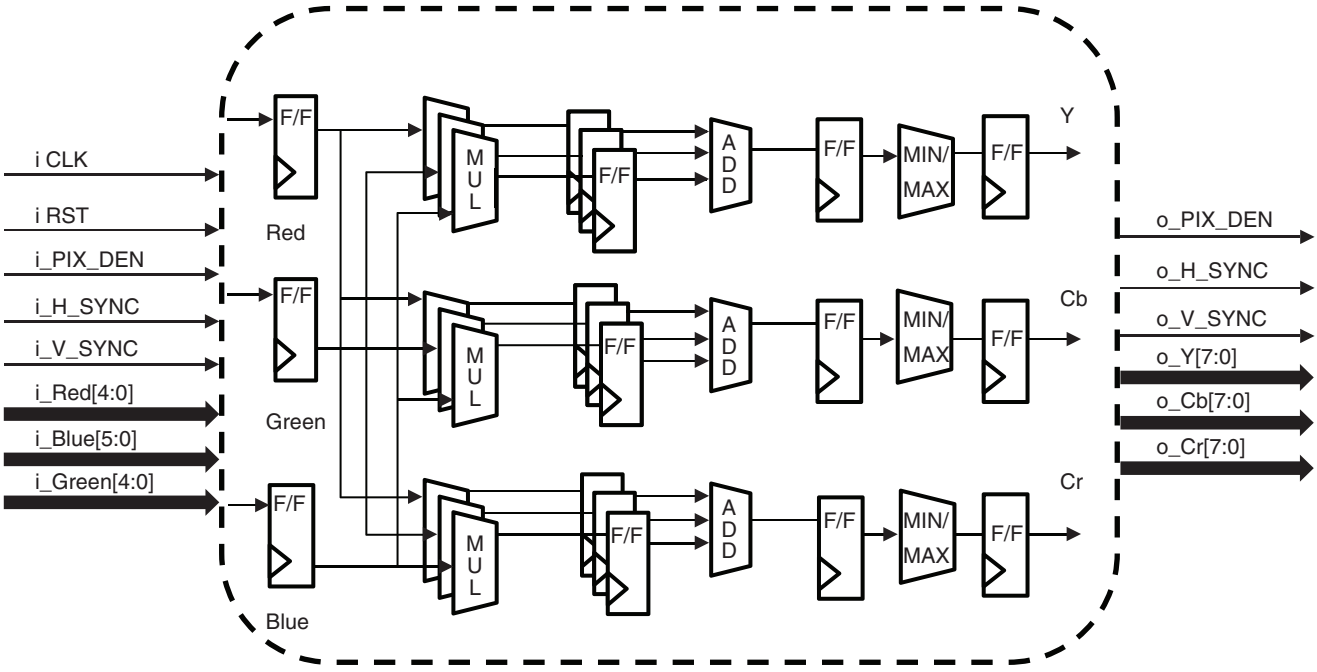
Signal Description

Table 1. Signal Description

Signal	Width	Type	Description
i_CLK	1	Input	Input Pixel Clock
i_RST	1	Input	Asynchronous Active High System Reset
i_PIX_DEN	1	Input	Data Enable (RGB valid) synchronized with pixel clock
i_H_SYNC	1	Input	Horizontal Sync
i_V_SYNC	1	Input	Vertical Sync
i_RED	5	Input	Red component of pixel
i_GREEN	6	Input	Green component of pixel
i_BLUE	5	Input	Blue component of pixel
o_PIX_DEN	1	Output	YCbCr valid data synchronized with pixel clock
o_H_SYNC	1	Output	Pipelined Horizontal Sync
o_V_SYNC	1	Output	Pipelined Vertical Sync
o_Y	8	Output	Converted Y component
o_Cb	8	Output	Converted Cb component
o_Cr	8	Output	Converted Cr component

Design Module Description

Figure 2. Functional Block Diagram



Configurable parameter

None

Register Map

This design does not have any user accessible registers or memory.

Design Details

This module converts RGB to YCbCr, consisting of one luma component(Y) representing brightness, and two chroma components (Cb and Cr) as per the following conversion expressions:

- Y = 16 + (0.2567890625 * Red) + (0.50412890625 * Green) + (0.09790625 * Blue)
- Cb = 128 + (0.14822265625 * Red) + (0.2909921875 * Green) + (0.43921484375 * Blue)
- Cr = 128 + (0.43921484375 * Red) + (0.3677890625 * Green) + (0.071442578125 * Blue)

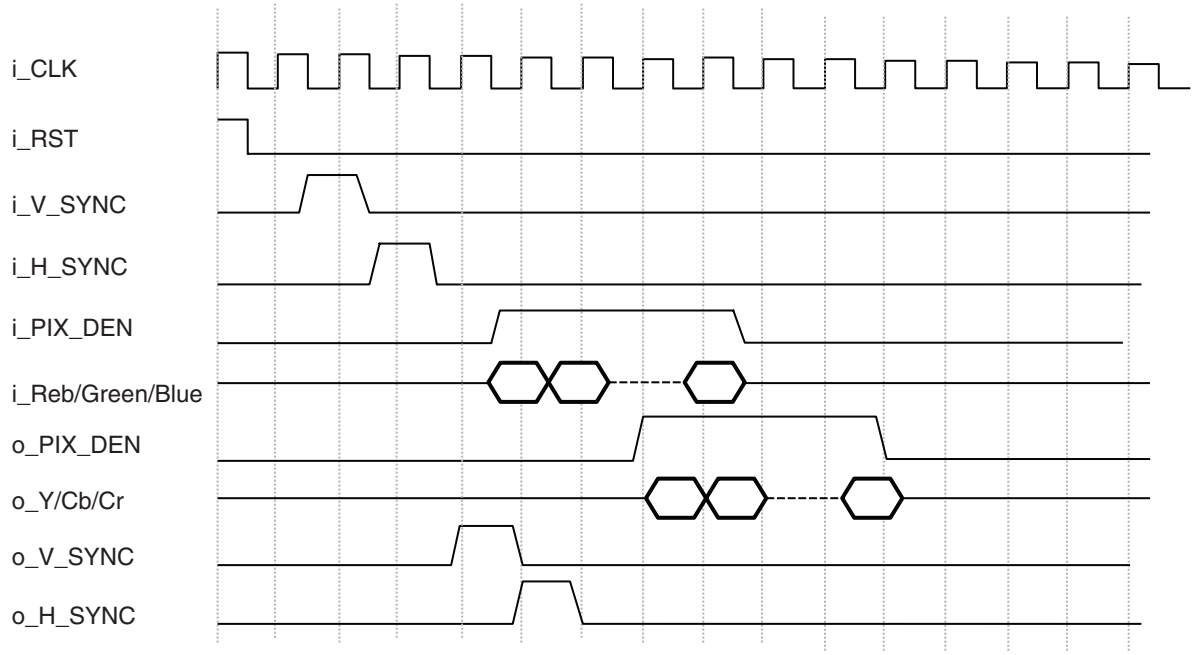
The implementation comprises of a set of constant coefficient multipliers implemented as shift and add adders. This is a fully synchronous design and all the modules listed in the block diagram generate registered outputs, clocked by input pixel clock. Considering the large amount of data path involved here, a pipelined implementation is provided to improve the performance. Computed Y, Cb and Cr values are clipped and limited to maximum/minimum permissible range. To facilitate easy insertion to practical video systems, the design conveniently pipelines the video control signals H_SYNC, V_SYNC, and DEN by introducing a latency of 5 clock cycles.

Initialization Conditions

This design does not have any user specific initialization conditions.

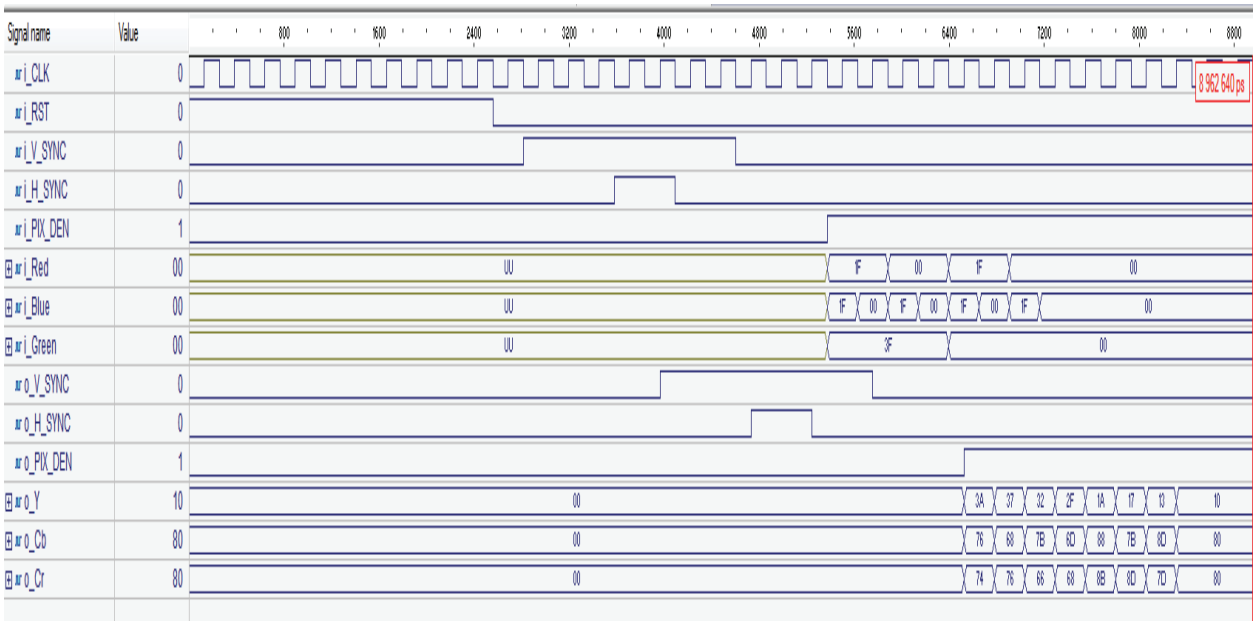
Timing Diagram

Figure 3. Timing Diagram



Simulation Waveforms

Figure 4. Simulation Waveforms



Usage Examples

RGB to YCbCr converters are useful in applications like JPEG and MPEG image encoders, which is used in DVDs, digital TV and Video CDs, where images are coded in YCbCr format. YCbCr is also the most preferred format for hue and saturation control of images.

Simulation setup comprises of a testbench which provides input RGB565 values for various colors like red, blue, green, white etc… The DUT generated output YCbCr 8-bit values are compared against the corresponding known YCbCr values.

Implementation

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Performance and Resource Utilization

Table 2. Performance and Resource Utilization

Family	Language	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architecture Resources
iCE40[1]	VHDL	318	>50	47	(74/160) PLBs

1. Performance and utilization characteristics are generated using iCE40-LP1K-CM121 with iCEcube2 design software.

References

- iCE40 Family Handbook

Technical Support Assistance

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Revision History

Date	Version	Change Summary
April 2013	01.0	Initial release.