LatticeECP3 Product Family Qualification Summary

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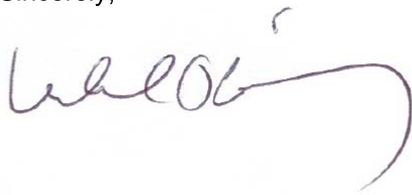
Dear Customer,

Welcome to the Lattice Semiconductor Corp. LatticeECP3 Product Family Qualification Report. This report reflects our continued commitment to product quality and reliability. The information in this report is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

This report is another member of a new generation of Product Qualification Summary Reports. The information contained in this document is extensive, and represents the entire qualification effort for this device family. Our goal is to provide this information to support your decision making process, and to facilitate the selection and use of our products.

As always, your feedback is valuable to Lattice. Our goal is to continuously improve our systems, including the generation of this report and the data included. Please feel free to forward your comments and suggestions to your local Lattice representative. We will use that feedback carefully and wisely in our effort to maximize customer satisfaction.

Sincerely,



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1.0 INTRODUCTION

The LatticeECP3 family is the third generation high value FPGA (Field Programmable Gate Array) from Lattice Semiconductor, which offers the industry's lowest power consumption and price of any SERDES-capable FPGA device. The LatticeECP3 FPGA family offers multi-protocol 3.2G SERDES with XAUI jitter compliance, DDR3 memory interfaces, powerful DSP capabilities, high density on-chip memory and up to 149K LUTS, all with half the power consumption of competitive SERDES-capable FPGAs. The entire LatticeECP3 family is manufactured using Fujitsu's advanced low power 65nm process technology.

The LatticeECP3 device family expands look-up-table (LUT) capacity to 149K logic elements and supports up to 486 user I/Os. The LatticeECP3 device family also offers up to 320 18x18 multipliers and a wide range of parallel I/O standards. The LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and multi-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

The LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media. Table 1.1 shows the LUTs, package and I/O options, along with other key parameters.

Table 1.1 LatticeECP3 Product Family Attributes

	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
EBR SRAM (Kbits)	552	1327	4420	4420	6850
EBR SRAM Blocks	30	72	240	240	372
Dist RAM (Kbits)	36	68	145	188	303
18x18 Multipliers	24	64	128	128	320
3.2Gbps SERDES Channels	4	4	12	12	16
Maximum Available I/O	222	310	490	490	586
PLLs + DLLs	2+2	4+2	10+2	10+2	10+2
Core Voltage	1.2V	1.2V	1.2V	1.2V	1.2V
Die Fabrication Site	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie
Process Technology	65 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS
Die Metallization	Cu	Cu	Cu	Cu	Cu
Die Interconnect Dielectric	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN
Packages – I/O	**SERDES I/O Combinations**				
256-ball ftBGA (17x17 mm)	4 / 133	4 / 133			
484-ball fpBGA (23x23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672-ball fpBGA (27x27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156-ball fpBGA (35x35 mm)			12 / 490	12 / 490	16 / 586

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2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITs. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Table 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The LatticeECP3 family is the third generation FPGA product family and first 65 nm (CS200A) SRAM Technology based product offering. The Lattice Semiconductor LatticeECP3 FPGA product family qualification efforts are based on the first LatticeECP3 devices in the family per the Lattice Semiconductor Qualification Procedure, doc#70-100164.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at www.latticesemi.com/lit/docs/qa/product_reliability_monitor.pdf .

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Figure 2.1: Lattice Standard Product Qualification Process Flow

This diagram represents the standard qualification flow used by Lattice to qualify new Product Families. The target end market for the Product Family determines which flow options are used. The LatticeECP3 Product Family was qualified using the Commercial / Industrial Qualification Option.

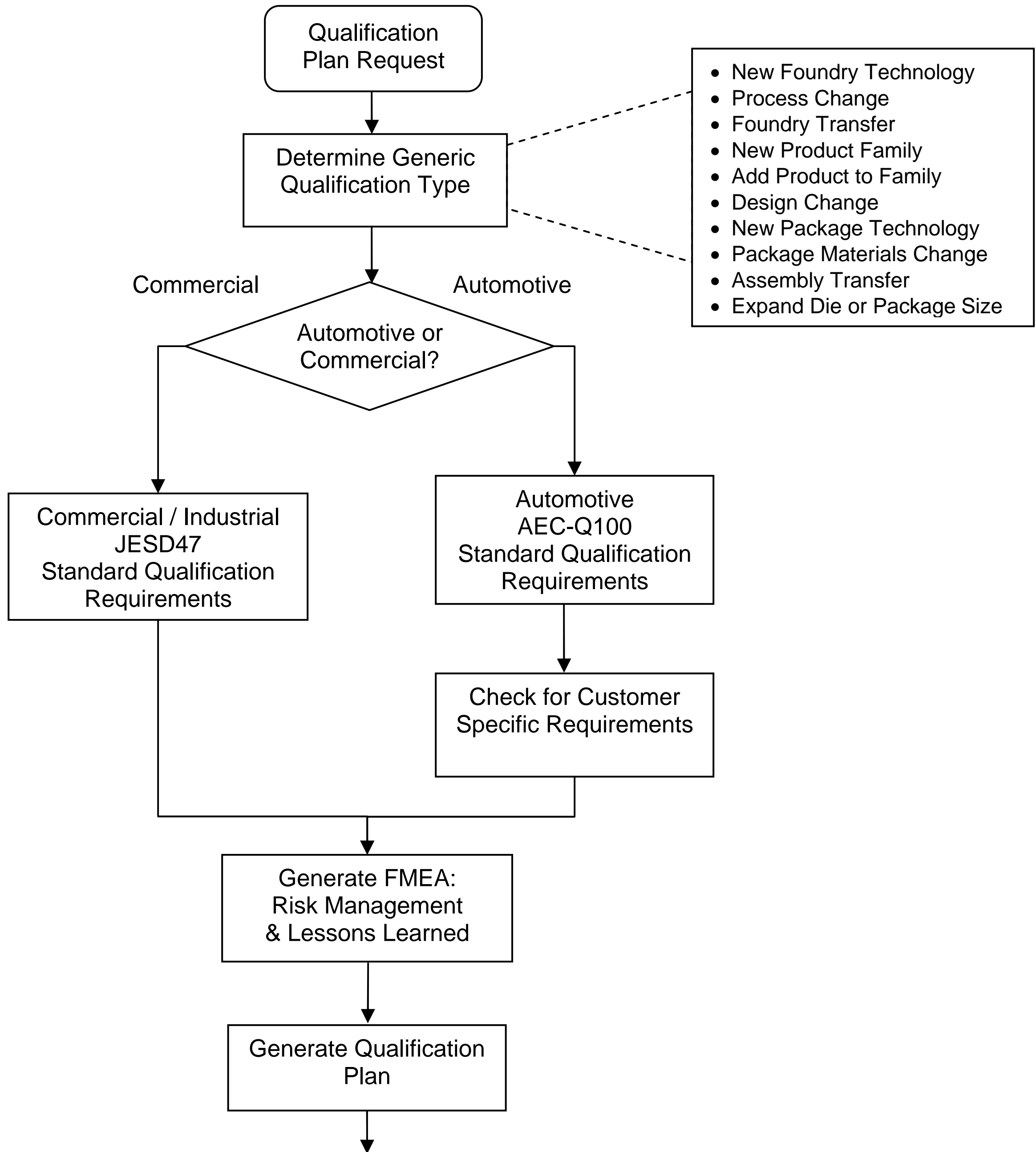

Figure 2.1: Lattice Standard Product Qualification Process Flow (cont.)

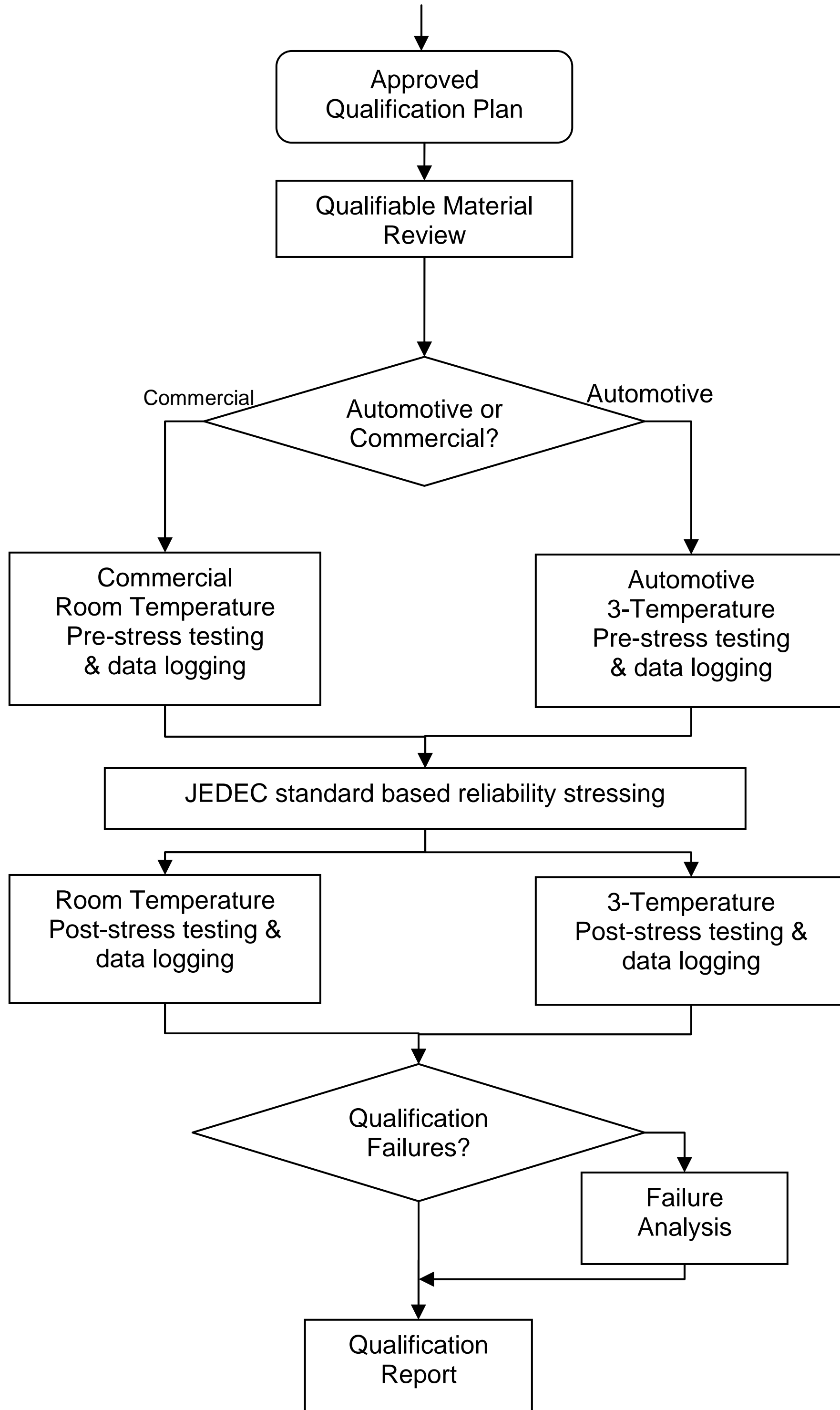

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Table 2.2: Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typical)	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 87-101943, MIL-STD-883, Method 1005.8, JESD22-A108C LatticeECP3	125° C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs.	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
High Temp Storage Life HTSL	Lattice Procedure # 87-101925, JESD22-A103C LatticeECP3	150° C, at 168, 500, 1000, 2000 hours.	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
ESD HBM	Lattice Procedure # 70-100844, MIL-STD-883, Method 3015.7 JESD22-A114E	Human Body Model	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD CDM	Lattice Procedure # 70-100844, JESD22-C101D	Charged Device model	3 parts/lot 1-2 lots typical	Design, Foundry Process
Latch Up Resistance LU	Lattice Procedure # 70-101570, JESD78A	±100 ma on I/O's, Vcc +50% on Power Supplies. (Max operating temp.)	6 parts/lot 1-2 lots typical	Design, Foundry Process
Surface Mount Pre-conditioning SMPC	Lattice Procedure # 70-103467, IPC/JEDEC J-STD-020D.1 JESD-A113F FPGA - MSL 3	10 Temp cycles, 24 hr 125° C Bake 192hr. 30/60 Soak 3 SMT simulation cycles	All units going into Temp Cycling, UHAST, BHAST, 85/85	Plastic Packages only
Temperature Cycling TC	Lattice Procedure #70-101568, MIL-STD- 883, Method 1010, Condition B JESD22-A104C	(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment	45 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification
Power Temperature Cycling PTC		(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment with asynchronous power on-off cycling.	45 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification. This test is required only for Automotive-qualified devices with maximum rated power $\geq$ 1 watt or DTJ $\geq$ 40ºC.
Unbiased HAST UHAST	Lattice Procedure # 70-104285 JESD22-A118	2 atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 parts/lot 2-3 lots	Foundry Process, Package Qualification Plastic Packages only

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typical)	PERFORMED ON
Moisture Resistance Temperature Humidity Bias 85/85 THBS or Biased HAST BHAST	Lattice Procedure # 70-101571, JESD22-A101B JESD22-A110B	Biased to maximum operating Vcc, 85° C, 85% Relative Humidity, 1000 hours or Biased to maximum operating Vcc, 2atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 devices/lot 2-3 lots	Design, Foundry Process, Package Qualification Plastic Packages only
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or applicable LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	Package Qualification
Ball Shear	Lattice Procedure # 70-104056 # 70-100433	Per Package Type	3 devices per package / 30 balls each unit	Package Qualification

3.0 QUALIFICATION DATA FOR 65nm PROCESS TECHNOLOGY

The LatticeECP3 family is the third generation FPGA product family and first 65nm (CS200A) SRAM Technology based product offering. The LatticeECP3 product family is used as the primary technology qualification vehicle.

Product Family: LatticeECP3
Packages offered: ftBGA, fpBGA
Process Technology Node: 65 nm

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3.1 LatticeECP3 Product Family Life Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 “Temperature, Bias, and Operating Life”, a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.
The Early Life Failure Rate (ELFR) test uses large samples sizes for a short duration (48 Hours) HTOL stress to determine the infant mortality rate of a device family.

LatticeECP3 Life Test (HTOL) Conditions:

Stress Duration: 48, 168, 500, 1000, 2000 hours.
Stress Conditions: LatticeECP3 (LFE3): V_{CC}=1.26V/ V_{CCIO}=3.47, $T_{JUNCTION}$ = 130°C
Stress Conditions Fujitsu Test Chip: (Test Chip x): V_{DD}=Max, $T_{JUNCTION}$ = 125°C
Method: Lattice Document # 87-101943 and JESD22-A108C

Table 3.1.1: LatticeECP3 Product Family Life Results

Product Name	Package	Lot #	Qty	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
LFE3-95E	BFN484	Lot #1	98		0	0	0	0	196,000
LFE3-95E	BFN484	Lot #2	98		0	0	0	0	196,000
LFE3-95E	BFN484	Lot #2	269	0					12,912
LFE3-95E	BFN484	Lot #3	856	0					41,088
LFE3-95E	BFN484	Lot #3	49		0	0	0	0	98,000
LFE3-150EA	BFN672	Lot #1	84		0	0	0	0	168,000
LFE3-150EA	BFN672	Lot #2	84		0	0	0	0	168,000
Test Chip 1[A]	QFP-120	Lot#1	77		0	0	0		77,000
Test Chip 2[B]	QFP-120	Lot #1	77		0	0	0	0	144,000
Test Chip 3[C]	QFP-120	Lot #1	77		0	0	0	0	144,000
Test Chip 4[D]	BGA-288	Lot #1	77		0	0	0	0	144,000
Test Chip 5[D]	BGA-288	Lot #2	77		0	0	0		77,000

A = Analog Circuit
B = 9Mbit SRAM
C = 4M Gates
D = SRAM + Logic

CS200A Cumulative Life Testing Device Hours = 1,496,000
CS200A Cumulative Result / Sample Size = 0 / 1,923
CS200A FIT Rate = 5 FIT
FIT Assumptions: CL=60%, AE=0.7eV, Tjref=55C

ECP3 HTOL (2000 Hrs) Cumulative Result / Sample Size = 0 / 413
ECP3 ELFR (48 Hrs) Cumulative Result / Sample Size = 0 / 1,125
Test Chip Cumulative Sample Size = 0 / 385

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3.2 LatticeECP3 Product Family – ESD and Latch UP Data

Electrostatic Discharge-Human Body Model:
LatticeECP3 product family was tested per the JESD22-A114E Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure and Lattice Procedure # 70-100844.
All units were tested at 25^0C and $+105^0$C prior to reliability stress and after reliability stress. No failures were observed within the passing classification

Table 3.2.1 LatticeECP3 ESD-HBM Data

Product Type	256-ftBGA	484-fpBGA	672-fpBGA	1156-fpBGA	Comments
LFE3-150EA			>1000V Jedec: Class 1C	>1000V Jedec: Class 1C	
LFE3-95EA		>1000V Jedec: Class 1C	>1000V Jedec: Class 1C	>1000V Jedec: Class 1C	
LFE3-70EA		>1000V Jedec: Class 1C	>1000V Jedec: Class 1C	>1000V Jedec: Class 1C	
LFE3-35EA	>1000V Jedec: Class 1C	>1000V Jedec: Class 1C	>1000V Jedec: Class 1C		
LFE3-17EA	>1000V Jedec: Class 1C	>1000V Jedec: Class 1C			

HBM classification for Commercial/Industrial products, per JESD22-A114E

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Electrostatic Discharge-Charged Device Model:

LatticeECP3 product family was tested per the JESD22-C101D, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure and Lattice Procedure # 70-100844.

All units were tested at room temperature 25^{0}C and ambient temperature 90^{0}C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.2 LatticeECP3 ESD-CDM Data

Product Type	256-ftBGA	484-fpBGA	672-fpBGA	1156-fpBGA	Comments
LFE3-150EA			>500V* Jedec: Class III	>500V* Jedec: Class III	*Except 400V< HDIN <450V Jedec: Class II
LFE3-95EA		>500V* Jedec: Class III	>500V* Jedec: Class III	>500V* Jedec: Class III	*Except 400V< HDIN <450V Jedec: Class II
LFE3-70EA		>500V* Jedec: Class III	>500V* Jedec: Class III	>500V* Jedec: Class III	*Except 400V< HDIN <450V Jedec: Class II
LFE3-35EA	>500V Jedec: Class III	>500V Jedec: Class III	>500V* Jedec: Class III		*Except 400V< HDIN <450V Jedec: Class II 672-fpBGA only
LFE3-17EA	>500V Jedec: Class III	>500V Jedec: Class III			All pins Jedec: Class III

CDM classification for Commercial/Industrial products, per JESD22-C101D

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Latch-Up:

LatticeECP3 product family was tested per the JEDEC EIA/JESD78A IC Latch-up Test procedure and Lattice Procedure # 70-101570.

All units were tested at room temperature 25^{0}C and ambient temperature 90^{0}C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.3 LatticeECP3 I/O Latch Up >100mA @ HOT (105°C) Data

Die Size	256-ftBGA	484-fpBGA	672-fpBGA	1156-fpBGA	Comments
LFE3-150EA			By Extension*	>+/-100mA	JESD78A, Class IIA, all I/O's
LFE3-95EA		By Extension*	By Extension*	>+/-100mA	JESD78A, Class IIA, all I/O's
LFE3-70EA		By Extension*	By Extension*	>+/-100mA	JESD78A, Class IIA, all I/O's
LFE3-35EA	By Extension*	By Extension*	>+/-100mA		JESD78A, Class IIA, all I/O's
LFE3-17EA	By Extension*	>+/-100mA			JESD78A, Class IIA, all I/O's

Table 3.2.4 LatticeECP3 Vcc Latch Up >1.5X @ HOT (105°C) Data

Die Size	256-ftBGA	484-fpBGA	672-fpBGA	1156-fpBGA	Comments
LFE3-150EA			By Extension*	>1.5X Vcc	JESD78A, Class IIA, all supplies
LFE3-95EA		By Extension*	By Extension*	>1.5X Vcc	JESD78A, Class IIA, all supplies
LFE3-70EA		By Extension*	By Extension*	>1.5X Vcc	JESD78A, Class IIA, all supplies
LFE3-35EA	By Extension*	By Extension*	>1.5X Vcc		JESD78A, Class IIA, all supplies
LFE3-17EA	By Extension*	>1.5X Vcc			JESD78A, Class IIA, all supplies

*All smaller packages for a given product are qualified by an extension.

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4.0 PACKAGE QUALIFICATION DATA FOR LatticeECP3 PRODUCT FAMILY

The LatticeECP3 product family is offered in ftBGA and fpBGA packages. This report details the package qualification results of the initial LatticeECP3 product introductions. Package qualification tests include Temperature Cycling (T/C), Un-biased HAST (UHAST), Biased HAST (BHAST) and High Temperature Storage (HTSL). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection.

The generation and use of generic data is applied across a family of products or packages emanating from one base wafer foundry or assembly process is a Family Qualification, or Qualification by Extension. For the package stresses BHAST, UHAST and HTSL, these are considered generic for a given Package Technology. T/C is considered generic up to an evaluated die size + package size + 10%, for a given Package Technology. Surface Mount Pre-Conditioning (SMPC) is considered generic up to an evaluated Peak Reflow temperature, for a given Package Technology. The following table demonstrates the package qualification matrix.

Table 4.0 Product-Package Qualification-By-Extension Matrix

<table>
<tr><th rowspan="2">Products</th><th rowspan="2">Stress Test</th><th colspan="4">Advanced Semiconductor Engineering, Malaysia (ASEM)</th></tr>
<tr><th>256-ftBGA</th><th>484-fpBGA</th><th>672-fpBGA</th><th>1156/1152-fpBGA</th></tr>
<tr><td rowspan="5">ECP3-150EA</td><td>SMPC</td><td colspan="2" rowspan="5">Packages not offered</td><td rowspan="5">(1) & (2)</td><td>MSL3 250°C</td></tr>
<tr><td>T/C</td><td>1000 cycles</td></tr>
<tr><td>BHAST</td><td>(2)</td></tr>
<tr><td>UHAST</td><td>(2)</td></tr>
<tr><td>HTSL</td><td>(2)</td></tr>
<tr><td rowspan="5">ECP3-95EA</td><td>SMPC</td><td rowspan="5">Package not offered</td><td rowspan="5">(2)</td><td rowspan="5">(2)</td><td>MSL3 250°C</td></tr>
<tr><td>T/C</td><td>1000 cycles</td></tr>
<tr><td>BHAST</td><td>96 hours</td></tr>
<tr><td>UHAST</td><td>96 hours</td></tr>
<tr><td>HTSL</td><td>1000 hours</td></tr>
<tr><td rowspan="5">ECP3-70EA</td><td>SMPC</td><td rowspan="5">Package not offered</td><td rowspan="5">(2)</td><td rowspan="5">(2)</td><td rowspan="5">(2)</td></tr>
<tr><td>T/C</td></tr>
<tr><td>BHAST</td></tr>
<tr><td>UHAST</td></tr>
<tr><td>HTSL</td></tr>
<tr><td rowspan="5">ECP3-35EA</td><td>SMPC</td><td>MSL3 260°C</td><td rowspan="5">(2)</td><td rowspan="5">(2)</td><td rowspan="5">Package not offered</td></tr>
<tr><td>T/C</td><td>1000 cycles</td></tr>
<tr><td>BHAST</td><td>(2)</td></tr>
<tr><td>UHAST</td><td>96 hours</td></tr>
<tr><td>HTSL</td><td>(2)</td></tr>
<tr><td rowspan="5">ECP3-17EA</td><td>SMPC</td><td rowspan="5">(3)</td><td rowspan="5">(2)</td><td colspan="2" rowspan="5">Packages not offered</td></tr>
<tr><td>T/C</td></tr>
<tr><td>BHAST</td></tr>
<tr><td>UHAST</td></tr>
<tr><td>HTSL</td></tr>
</table>

Notes:

1 – Largest die & largest package T/C extension testing covers all fpBGA package products in the LatticeECP3 family.

2 – Qualified by extension from LatticeECP3-95, BFN1152/BFN1156 testing.

3 – Qualified by extension from a combination of LatticeECP3-35EA, 256ftBGA and LatticeECP3-95, BFN1152/BFN1156 testing.

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4.1 LatticeECP3 Product Family Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JEDEC JESD22-A113F "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

Surface Mount Preconditioning (MSL3)
(10 Temperature Cycles, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, 250 °C Reflow Simulation, 3 passes) performed before all package tests.
MSL3 Packages: fpBGA, ftBGA
Method: Lattice Procedure # 70-103467, J-STD-020D.1 and JESD22-A113F

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LFE3-35EA	FTN256	ASEM	Lot #1	154	0	260°C
LFE3-35EA	FTN256	ASEM	Lot #2	154	0	260°C
LFE3-35EA	FTN256	ASEM	Lot #3	154	0	260°C
LFE3-95E	FN1152	ASEM	Lot #1	275	0	250°C
LFE3-95E	FN1152	ASEM	Lot #2	137	0	250°C
LFE3-95E	FN1152	ASEM	Lot #3	182	0	250°C
LFE3-95E	FN1152	ASEM	Lot #4	23	0	250°C
LFE3-95E	FN1152	ASEM	Lot #5	122	0	250°C
LFE3-95E	FN1152	ASEM	Lot #6	235	0	250°C
LFE3-95E	FN1152	ASEM	Lot #7	29	0	250°C
LFE3-95E	FN1152	ASEM	Lot #8	49	0	250°C
LFE3-95E	FN1152	ASEM	Lot #9	49	0	250°C
LFE3-95E	FN1156	ASEM	Lot #1	90	0	250°C
LFE3-95E	FN1156	ASEM	Lot #2	90	1*	250°C
LFE3-150EA	FN1156	ASEM	Lot #1	101	0	250°C
LFE3-150EA	FN1156	ASEM	Lot #2	101	0	250°C
LFE3-150EA	FN1156	ASEM	Lot #3	77	0	250°C

*1 failure for assembly defect
FAR#: 1380

Cumulative SMPC Failure Rate ECP3 = 1 / 2,022

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4.2 LatticeECP3 Product Family Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104 “Temperature Cycling”, Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: fpBGA, ftBGA
Stress Duration: 1000 cycles
Stress Conditions: Temperature cycling between -55°C to 125°C
Method: Lattice Procedure # 70-101568 and JESD22-A104C, Condition B

Table 4.2.1: Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Quantity	250 Cycles	500 Cycles	1000 Cycles
LFE3-35EA	FTN256	ASEM	Lot #1	77	0	0	0
LFE3-35EA	FTN256	ASEM	Lot #2	77	0	0	0
LFE3-35EA	FTN256	ASEM	Lot #3	77	0	0	0
LFE3-95E	FN1152	ASEM	Lot #1	77	0	0	0
LFE3-95E	FN1152	ASEM	Lot #2	77	0	0	0
LFE3-95E	FN1152	ASEM	Lot #3	77	0	0	0
LFE3-95E	FN1156	ASEM	Lot #1	45	0	0	0
LFE3-95E	FN1156	ASEM	Lot #2	44	0	0	0
LFE3-150EA	FN1156	ASEM	Lot #1	77	0	0	0
LFE3-150EA	FN1156	ASEM	Lot #2	77	0	0	0
LFE3-150EA	FN1156	ASEM	Lot #3	77	0	0	0

Cumulative Temp Cycle Failure Rate ECP3 = 0 / 782

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4.3 LatticeECP3 Product Family Power-Temperature Cycling Data

The Power and Temperature Cycling (PTC) test is no longer a JESD47 qualification requirement for Commercial and Industrial grade products. However, in the interest of excellence PTC was performed with modest sample sizes to determine the ability of this device to withstand alternate exposures at high and low temperature extremes and simultaneously the operating biases are periodically applied and removed. It is intended to simulate worst case conditions encountered in application environments. Devices are tested at 25°C after exposure to repeated cycling between -45°C to +85°C in an air environment consistent with JEDEC JESD22-A105C "Power-Temperature Cycling", Condition A temperature cycling requirements. Prior to Power and Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: fpBGA
Stress Duration: 1000 cycles
Stress Conditions: Temp cycling -45°C to +85°C, plus asynchronous power cycling =VCC=1.26V / VCCIO=3.47
Method: JESD22-A105C, Condition A

Table 4.3.1: Power-Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Quantity	250 Cycles	500 Cycles	1000 Cycles
LFE3-150EA	FN1156	ASEM	Lot #1	24	0	0	0
LFE3-150EA	FN1156	ASEM	Lot #2	24	0	0	0

Cumulative Power Temp Cycle Failure Rate ECP3 = 0 / 48

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4.4 LatticeECP3 Product Family Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent with JEDEC JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," the Unbiased HAST conditions are either 96 hours exposure at 130°C and 85% relative humidity (Condition A), or 264 hours exposure at 110°C and 85% relative humidity (Condition B). Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: ftBGA, fpBGA
Stress Duration: 96 Hrs (Condition A) or 264 Hrs (Condition B)
Stress Conditions: 130°C and 85% RH (Condition A) or 110°C and 85% RH (Condition B)
Method: Lattice Procedure # 70-104285 and JESD22-A118

Table 4.4.1: Unbiased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Temperature	Stress Duration
LFE3-35EA	FTN256	ASEM	Lot #1	77	0	110°C	264 Hrs
LFE3-35EA	FTN256	ASEM	Lot #2	77	0	110°C	264 Hrs
LFE3-35EA	FTN256	ASEM	Lot #3	77	0	110°C	264 Hrs
LFE3-95E	FN1152	ASEM	Lot #1	44	0	130°C	96 Hrs
LFE3-95E	FN1152	ASEM	Lot #2	30	0	130°C	96 Hrs
LFE3-95E	FN1152	ASEM	Lot #3	30	0	130°C	96 Hrs
LFE3-95E	FN1152	ASEM	Lot #4	23	0	130°C	96 Hrs
LFE3-95E	FN1152	ASEM	Lot #5	43	0	130°C	96 Hrs
LFE3-95E	FN1152	ASEM	Lot #6	50	0	130°C	96 Hrs

Cumulative Unbiased HAST failure Rate ECP3 = 0 / 451

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4.5 LatticeECP3 Product Family THB: Biased HAST Data

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD22-A110B "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are with Vcc bias and alternate pin biasing in an ambient of 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: ftBGA, fpBGA
Stress Conditions: Vcc= 1.26V/ V_{CCIO} = 3.3V, 130°C / 85% RH, 15 psig
Stress Duration: 96 hours
Method: Lattice Procedure # 70-101571 and JESD22-A110B

Table 4.5.1: Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LFE3-95E	FN1152	ASEM	Lot #1	77	0	96 Hrs
LFE3-95E	FN1152	ASEM	Lot #3	45	0	96 Hrs
LFE3-95E	FN1152	ASEM	Lot #5	32	0	96 Hrs
LFE3-95E	FN1152	ASEM	Lot #6	138	0	96 Hrs
LFE3-95E	FN1152	ASEM	Lot #7	29	0	96 Hrs
LFE3-95E	FN1152	ASEM	Lot #8	49	0	96 Hrs
LFE3-95E	FN1152	ASEM	Lot #9	49	0	96 Hrs
LFE3-95E	FN1156	ASEM	Lot #1	45	0	96 Hrs
LFE3-95E	FN1156	ASEM	Lot #2	45	0	96 Hrs

Cumulative BHAST failure Rate ECP3 = 0 / 509

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4.6 LatticeECP3 Product Family High Temperature Storage Life (HTSL)

High Temperature Storage Life (HTSL)

The High Temperature Storage Life test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. Consistent with JEDEC JESD22-A103C, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours. Prior to High Temperature Storage, all LatticeECP3 devices are subjected to Surface Mount Preconditioning as mentioned in Table 4.1.1. This is a relatively new requirement consistent with JESD47F for Pb-free, wirebonded packages.

MSL3 Packages: ftBGA, fpBGA
Stress Duration: 168, 500, 1000 hours.
Temperature: 150°C (ambient)
Method: Lattice Document # 87-101925 and JESD22-A103C / JESD22-A117A

Table 4.6.1: LatticeECP3 High Temperature Storage Life Results

Product Name	Package	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LFE3-95E	FN1152	Lot #1	77	0	0	0	77000
LFE3-95E	FN1152	Lot #2	30	0	0	0	30000
LFE3-95E	FN1152	Lot #3	30	0	0	0	30000
LFE3-95E	FN1152	Lot #4	47	0	0	0	47000
LFE3-95E	FN1152	Lot #5	47	0	0	0	47000

ECP3 Cumulative HTSL Failure Rate = 0 / 231
ECP3 Cumulative HTSL Device Hours = 231,000

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5.0 LatticeECP3 Process Reliability Wafer Level Review

Several key fabrication process related parameters have been identified by the foundry that would affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. Normal operating conditions are defined in the Electrical Design Rules (EDR). These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence.

Table 5.1 – Wafer Level Reliability Results

HCI

Device	LVN	LVP	HVN	HVP
delta Ids	-10%	-10%	-10%	-10%
Celsius	25	25	25	25
Vgstress	Vd	Vd	Vd/2	Vd/2
Vds	1.26	-1.26	3.465	-3.465
TTF	3 lots>33yr	3 lots>1500yr	4 lots>24.8yr	3 lots>1600yr

TDDB

Device	LVN	LVP	HVN	HVP	Intermediate IMD	Semi-Global IMD
Celsius	125	125	125	125	125	125
Vg	1.26	-1.26	3.465	-3.465	3.465	3.465
Max Area	0.75cm^2	1.0cm^2	0.2cm^2	0.5cm^2	L/S=66nm	L/S=117nm
0.1% TTF	3 lots>10k yr	3 lots>16k yr	3 lots>540yr	3 lots>275yr	6 lots>39yr *	3 lots>2500 yr *

NBTI

Device	LVP	HVP
delta Vth	50mv	100mv
Celsius	125	125
Vg	-1.26	-3.465
TTF	3 lots>490yr	3 lots>48yr

EML

Device	Intermediate	Intermediate	Semi-Global	Global	Top Al
Celsius	125	125	125	125	125
delta R	+5%	+5%	+5%	+5%	+5%
Jmax	1.70e5A/cm^2	1.70e5A/cm^2	2.41e5A/cm^2	3.61Ae5/cm^2	2.5e5A/cm^2
0.1% TTF	3 lots>12yr	3 lots>450yr *	3 lots>29yr	3 lots>12yr	3 lots>19yr

SM

Device	Intermediate	Semi-Global	Global
delta R	+100%	+100%	+100%
Celsius	125	125	125
TTF	6 lots>900yr *	3 lots>123yr	3 lots>4000yr

Note: * Includes data with new inter-metal dielectric (IMD).
Note: Reliability life times are based on listed temperature and used conditions. Detailed WLR test conditions are available upon request.

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6.0 LatticeECP3 Soft Error Rate Data

Soft Error Rate testing is conducted to characterize the sensitivity of SRAM storage and device logic elements to High Energy Neutron and Alpha Particle radiation. Charge induced by the impact of these particles can collect at sensitive nodes in the device, and result in changes in the internal electrical states of the device. While these changes do not cause physical damage to the device, they can cause a logical error in device operation.

All testing conforms to JEDEC JESD-89.

Table 6.1 - LatticeECP3 MEASURED FITs / Mb

Stress / Structure	CONFIGURATION BITS	EBR BITS
Neutron	324	611
Alpha	138	363

Note: Detailed SER data is available upon request.

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7.0 LatticeECP3 PACKAGE ASSEMBLY INTEGRITY TESTS

7.1 Solder Ball Shear

This test is used to measure the shear strength of a ball bond's adhesion to the bond pad.

Table 7.1.1 Solder Ball Shear Data for LatticeECP3 fpBGA Packages

Attributes	484- fpBGA	672-fpBGA	1156-fpBGA
Number of Units Tested	3	3	3
Number of Tests / Unit	30	30	30
Total Number of Tests	90	90	90
Minimum Load	835.9 gram	810.7 gram	825.7 gram
Maximum Load	1171.2 gram	1150.9 gram	1199.2 gram
Min Cpk	>5.83	>3.75	>3.65

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8.0 LatticeECP3 ADDITIONAL FAMILY DATA

Table 8.1: LatticeECP3 Package Assembly Data – fpBGA

Package Attributes / Assembly Sites	ASEM
Die Family (Product Line)	ECP3
Fabrication Process Technology	65nm CMOS (CS200A)
Package Assembly Site	Malaysia
Package Type	fpBGA
Ball Counts	484/672/1152/1156
Die Preparation/Singulation	wafer saw, full cut
Die Attach Material	Ablebond 2100A
Mold Compound Supplier/ID	Hitachi 9750HF Series
Wire Bond Material	Gold (Au)
Wire Bond Methods	Thermosonic Ball
Substrate Material	Bismaleimide Triazine HL83X Series
Lead Finish Plating or BGA Ball	Sn96.5/Ag3.0/Cu0.5
Marking	Laser

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