Lattice ispCLOCK Product Family Qualification Summary

Lattice Document # 25 - 106041 July 2009

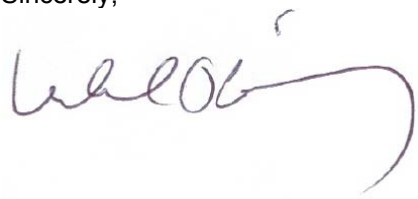
Dear Customer,

Welcome to the Lattice Semiconductor Corp. ispCLOCK Product Family Qualification Report. This report reflects our continued commitment to product quality and reliability. The information in this report is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

This is the first of a new generation of Product Qualification Summary Reports. The information contained in this document is extensive, and represents the entire qualification effort for this device family. Our goal is to provide this information to support your decision making process, and to facilitate the selection and use of our products.

As always, your feedback is valuable to Lattice. Our goal is to continuously improve our systems, including the generation of this report and the data included. Please feel free to forward your comments and suggestions to your local Lattice representative. We will use that feedback carefully and wisely in our effort to maximize customer satisfaction.

Sincerely,



Michael J. Gariepy
VP – Reliability and Quality Assurance

LATTICE SEMICONDUCTOR CORP.

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1.0 INTRODUCTION

The ispCLOCK family devices are in-system-programmable high-fanout PLL-based clock drivers designed for use in high performance communications and computing applications. The ispCLOCK product portfolio includes the ispCLK5300S, ispCLK5400D and ispCLK5600AV families. These devices offer multiple single-ended or differential clock outputs. Outputs may be independently configured to support I/O standards (LVDS, LVPECL, LVTTL, LVCMOS, SSTL, HSTL) and generate multiple output frequencies. All configuration information is stored on-chip in nonvolatile E2CMOS memory. For complete device details refer to the appropriate ispClock product data sheet. This report details the reliability qualification results for the ispClock device families.

The ispCLOCK Product Family is built on Lattice Semiconductor's 1.8V/2.5V/3.3V UM10 process. UM10 is a shallow trench isolated, 0.22 um CMOS process with Electrically Erasable cell (E^2 Cell) modules. This process uses five planarized metal interconnect layers and a single layer polysilicon. UM10 is manufactured at Seiko Epson Corporation. To verify product reliability, Lattice Semiconductor maintains an active Early Life and Inherent Life Reliability Monitor program on the ispCLOCK products. Lattice Semiconductor publishes the Reliability Monitor Data quarterly.

Table 1.1 Lattice ispCLOCK Product Family Attributes

Features	ispCLOCK 5600A Family	ispCLOCK 5400D Family	ispCLOCK 5300S Family
Device Types	CLK5620A CLK5610A	CLK5410D CLK5406D	CLK5320S, CLK5316S, CLK5312S, CLK5308S, CLK5304S
Outputs	20 or 10	10 or 6	20, 16, 12, 8, or 4
Input Operating Frequency Range	8 to 400MHz	50 to 400MHz	8 to 267MHz
Output Operating Frequency Range	4 to 400MHz	50 to 400MHz	5 to 267MHz
VCO Operation	320 to 800MHz	400 TO 800MHz	160 to 400MHz
Spread Spectrum Compatibility	Yes	Yes	Yes
Single-Ended Fan-out Buffer Interfaces	LVTTL, LVCMOS, HSTL, eHSTL, SSTL	None	LVTTL, LVCMOS, HSTL, eHSTL, SSTL
Single-Ended Clock Reference and Feedback Interfaces	LVTTL, LVCMOS, SSTL, HSTL	LVCMOS	LVTTL, LVCMOS, HSTL, eHSTL, SSTL
Differential Fan-out Buffer Interfaces	SSTL, HSTL, LVDS, LVPECL	LVDS, LVPECL, HSTL, SSTL, HCSL, MLVDS	None
Differential Clock Reference and Feedback Interfaces	HSTL, SSTL, LVDS, LVPECL	LVDS, LVPECL, HSTL, SSTL, HCSL	LVDS, LVPECL, HSTL, SSTL
Type of PLL Feedback	Internal/External	Internal/External	Internal/External
M, N Dividers	Count from 1 to 40	None	None
Number of V Dividers	5	4	3
V Divider Count Range	2 to 80 (in steps of 2)	2 to 16 (in powers of 2)	1 to 32 (in powers of 2)
Maximum Cycle-Cycle Jitter	70ps (peak-peak)	29ps (peak-peak)	70ps (peak-peak)
Maximum Period Jitter (RMS)	12ps	2.5ps	12ps
Maximum Phase Jitter (RMS)	50ps	6ps Typ.	50ps
Maximum Static Phase Offset	-100ps to 200ps	-5ps to 95ps	-40ps to 100ps
Frequencies Generated	5	4	3
Programmable Phase Skew	156ps to 12ns	156ps to 9.3ns	156ps to 5ns
Programmable Time Skew	None	0ps to 270ps	None
Fan-out Buffer Mode	No	Yes	Yes
Programmable Termination	40 to 70Ω & 20Ω Setting	None	40 to 70Ω & 20Ω Setting
Supply Voltage	3.3V	3.3V	3.3V
Process Technology	0.22um CMOS	0.22um CMOS	0.22um CMOS
Die Metallization	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu
Die Interconnect Dielectric	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS
Pins/Packages	48 TQFP 100 TQFP (Pb and Pb-Free)	48 QFNs 64 QFNs (Pb-Free)	48 TQFP 64 TQFP (Pb and Pb-Free)

2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITS. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Tables 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The ispCLOCK Product Family is built on Lattice Semiconductor's 1.8V/2.5V/3.3V UM10 process. UM10 is a shallow trench isolated 0.22um CMOS process with Electrically Erasable cell (E^2 Cell) modules. This process uses five planarized metal interconnect layers and a single layer polysilicon. UM10 is manufactured at Seiko Epson Corporation. To verify product reliability, Lattice Semiconductor maintains an active Early Life and Inherent Life Reliability Monitor program on the ispCLOCK products.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at www.latticesemi.com/lit/docs/qa/product_reliability_monitor.pdf .

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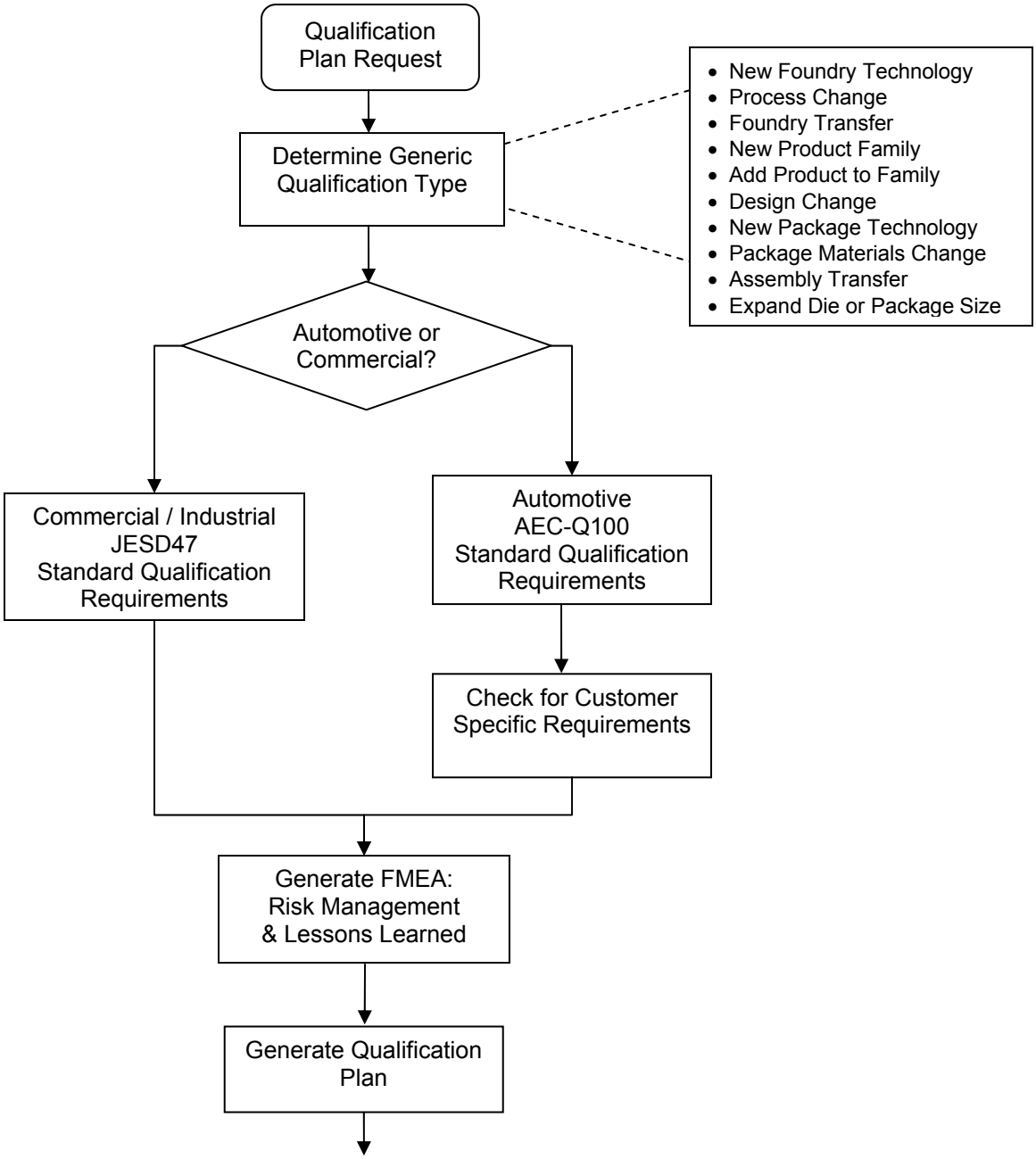
Figure 2.1: ispCLOCK Product Qualification Process Flow



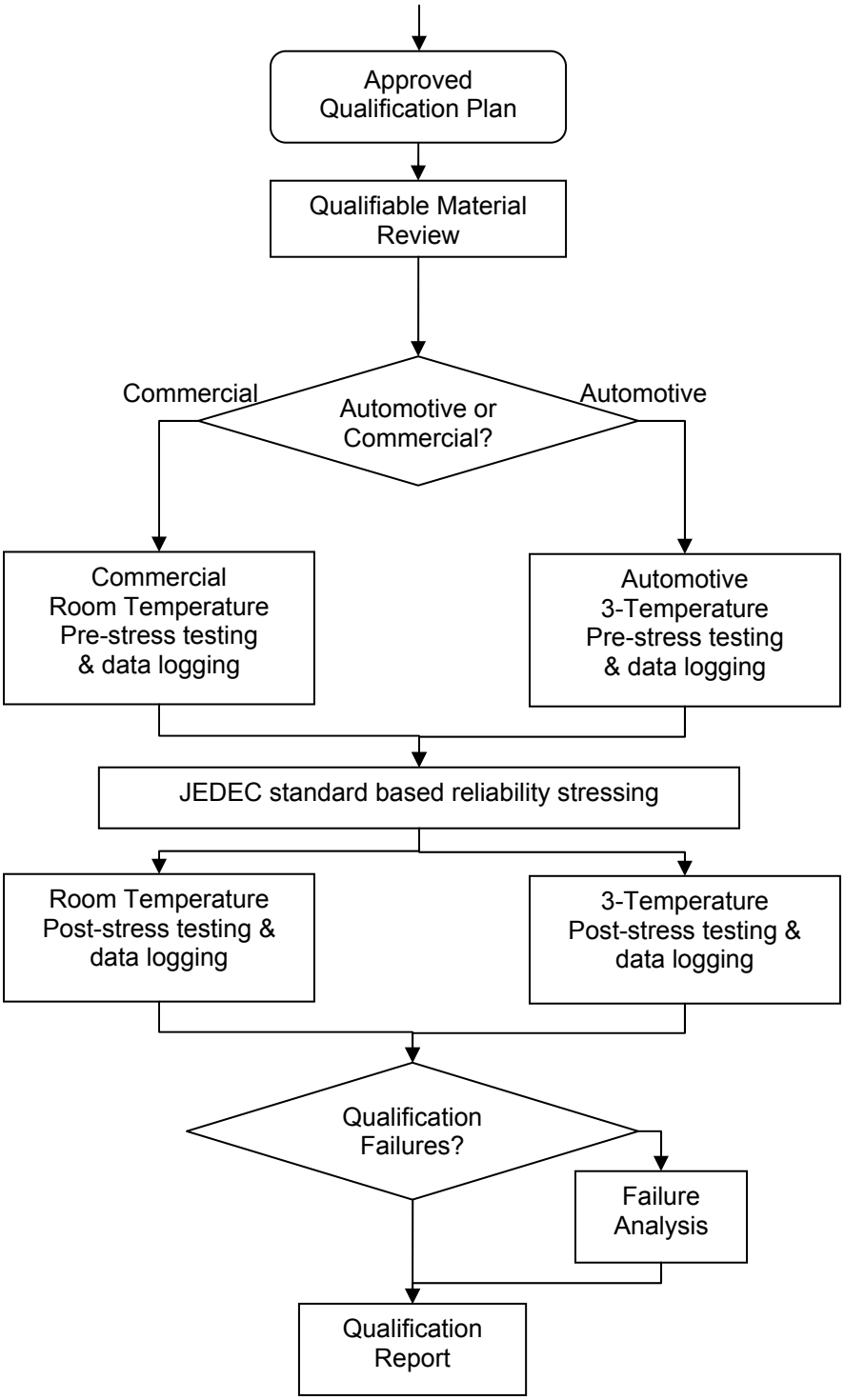


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Table 2.2: Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 87-101943, MIL-STD-883, Method 1005.8, JESD22-A108C ispCLOCK	125° C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs. Preconditioned with 1000 read/write cycles	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
High Temp Data Retention HTRX	Lattice Procedure # 87-101925, JESD22-A103C JESD22-A117A ispCLOCK	150° C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs. Preconditioned with 1000 read/write cycles	100/lot 2-3 lots	Design, Foundry Process, Package Qualification E^2 Cell Products Flash based Products
High Temp Storage Life HTSL	Lattice Procedure # 87-101925, JESD22-A103C ispCLOCK	150° C, at 168, 500, 1000, 2000 hours.	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
Endurance - Program/Erase Cycling Flash based Products	Lattice Procedure, # 70-104633 JESD22-A117A	Program/Erase devices to 100,000 cycles Program/Erase devices to 10X cycles of data sheet specification	10/lot 2-3 lots typical	Design, Foundry Process, Package Qualification. Not Applicable to ispCLOCK devices.
ESD HBM	Lattice Procedure # 70-100844, MIL-STD-883, Method 3015.7 JESD22-A114E	Human Body Model (HBM) sweep to 2000 volts – (130nm and older)	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD CDM	Lattice Procedure # 70-100844, JESD22-C101D	Charged Device model (CDM) sweep to 1000 volts (130nm and older)	3 parts/lot 1-3 lots typical	Design, Foundry Process
Latch Up Resistance LU	Lattice Procedure # 70-101570, JESD78A	±100 ma on I/O's, Vcc +50% on Power Supplies. (Max operating temp.)	6 parts/lot 1-3 lots typical	Design, Foundry Process
Surface Mount Pre-conditioning SMPC	Lattice Procedure # 70-103467, IPC/JEDEC J-STD-020D.1 JESD-A113F CPLD/FPGA - MSL 3	10 Temp cycles, 24 hr 125° C Bake 192hr. 30/60 Soak 3 SMT simulation cycles	All units going into Temp Cycling, UHAST, BHAST, 85/85	Plastic Packages only
Temperature Cycling TC	Lattice Procedure #70-101568, MIL-STD- 883, Method 1010, Condition B JESD22-A104C	(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment	45 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification
Unbiased HAST UHAST	Lattice Procedure # 70-104285 JESD22-A118	2 atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 parts/lot 2-3 lots	Foundry Process, Package Qualification Plastic Packages only

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
Moisture Resistance Temperature Humidity Bias 85/85 THBS or Biased HAST BHAST	Lattice Procedure # 70-101571, JESD22-A101B JESD22-A110B	Biased to maximum operating Vcc, 85° C, 85% Relative Humidity, 1000 hours or Biased to maximum operating Vcc, 2atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 devices/lot 2-3 lots	Design, Foundry Process, Package Qualification Plastic Packages only
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or applicable LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	Package Qualification
Wire Bond Strength	Lattice Procedure # 70-100220	Per package type	15 devices per pkg. per year	Design, Foundry Process, Package Qualification
Solderability	Lattice Procedure # 70-100212, MIL-STD-883, Method 2003	Steam Pre-conditioning 4-8 hours. Solder dip at 245°C+5°C	22 leads/ 3 devices/ Package family	All packages except BGAs

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3.0 QUALIFICATION DATA FOR ispCLOCK Product Family

The ispCLOCK Product Family is built on Lattice Semiconductor's 1.8V/2.5V/3.3V UM10 process. UM10 is a shallow trench isolated, 0.22 um CMOS process with Electrically Erasable cell (E^2 Cell) modules. This process uses five planarized metal interconnect layers and a single layer polysilicon. UM10 is manufactured at Seiko Epson Corporation. To verify product reliability, Lattice Semiconductor maintains an active Early Life and Inherent Life Reliability Monitor program on the ispCLOCK products.

Product Family: ispCLOCK5600A, ispCLOCK5400D, ispCLOCK5300S
Packages offered: TQFP, QFNs
Process Technology Node: 0.22um CMOS

3.1 ispCLOCK Product Family Life Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 “Temperature, Bias, and Operating Life”, a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

UM10 Life Test (HTOL) Conditions:

Stress Duration: 168, 500, 1000, 2000 hours.
Temperature: 125°C
Stress Voltage ispCLOCK: V_{CC}= 3.6V
Preconditioned with 1000 read/write cycles
Method: Lattice Document # 87-101943 and JESD22-A108

Table 3.1.1: UM10 Product Family HTOL Results

Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
ispPAC-CLK5312	Seiko	Lot #1	77	0	0	0	0	154000
ispPAC-CLK5312	Seiko	Lot #2	76	0	0	0	0	152000
* ispPAC-CLK5520	Seiko	Lot #1	72	0	0	0	0	144000
* ispPAC-CLK5520	Seiko	Lot #2	71	0	0	0	0	142000
* ispPAC-CLK5620	Seiko	Lot #1	76	0	0	0	0	152000
ispPAC-CLK5620A	Seiko	Lot #1	77	0	0	0	0	154000
ispPAC-CLK5410D	Seiko	Lot #1	77	0	0	0		77000
ispPAC-CLK5410D	Seiko	Lot #2	77	0	0	0		77000

* Development vehicle used for qualification.
Product not offered for sale.

UM10 Cumulative Device Hours = 1,052,000
UM10 Cumulative Sample Size = 0 / 603
Um10 FIT Rate = 11 FIT

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Low Temperature Operating Life (LTOL) Test

The Low Temperature Operating Life test is used to accelerate transistor performance degradation due to hot electron effects. A pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at V_{CC} 3.6 V and -55°C.

UM10 Life Test (LTOL) Conditions:

Stress Duration: 168, 500, 1000 hours.
Stress Conditions ispCLOCK: V_{CC}= 3.6V
Temperature = -55°C
Method: Lattice Document # 87-101943 and JESD22-A108

Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
* ispPAC-CLK5520	Seiko	Lot #1	73	0	0	0	73000

* Development vehicle used for qualification.
Product not offered for sale.

UM10 Cumulative Device Hours = 73,000
UM10 Cumulative Sample Size = 0 / 73

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3.2 ispCLOCK Product Family High Temperature Data Retention (HTRX) and High Temperature Storage Life (HTSL) Data

High Temperature Data Retention (HTRX)

The High Temperature Data Retention test measures the Electrically Erasable cell (E^2 cell) reliability while the High Temperature Operating Life test is structured to measure functional operating circuitry failure mechanisms. The High Temperature Data Retention test is specifically designed to accelerate charge gain on to or charge loss off of the floating gates in the device's array. Since the charge on these gates determines the actual pattern and function of the device, this test is a measure of the reliability of the device in retaining programmed information. In High Temperature Data Retention, the E^2 cell reliability is determined by monitoring the cell margin after biased static operation at 150°C. All cells in all arrays are life tested in both programmed and erased states.

The High Temperature Storage Life (HTSL) test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. For the non-volatile based products, the HTRX and HTSL stress and test conditions condition are the same. The HTSL test is covered by HTRX.

UM10 Data Retention (HTRX) Conditions:
Stress Duration: 168, 500, 1000, 2000 hours.
Temperature: 150°C
Stress Voltage ispCLOCK: V_{CC} = 3.6 V
Method: Lattice Document # 87-101925 and JESD22-A103 / JESD22-A117

Table 3.2.1: UM10 High Temperature Data Retention Results

Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
ispPAC-CLK5620A	Seiko	Lot #1	100	0	0	0	0	200000

UM10 Cumulative HTRX Failure Rate = 0 / 100
UM10 Cumulative HTRX Device Hours = 200,000

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High Temperature Storage Life (HTSL)

High Temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices. Units were stressed per JESD22-A103C, High Temperature Storage Life.

The High Temperature Storage Life units were stressed at 150°C.

The generation and use of generic data is applied across a family of products or packages emanating from one base wafer foundry or assembly process is a Family Qualification, or Qualification by Extension. Consistent with Lattice Semiconductor Corp. document # 25-100164, package reliability testing can be qualified by extension. Once a package outline is qualified within a package grouping as per doc #70-103639, all lower lead count (and smaller body size) packages within that package type and assembly technology are qualified by extension. Additionally, once an assembly technology has been qualified for one package type, that package type shall be qualified by extension to all future fabrication processes as long as those processes continue to use the same critical elements. Those critical elements in this case, are that the fab-process to fab-process pad metallization and passivation material. For the package stress HTSL, the critical elements for the qualification vehicle used are considered equivalent.

High Temperature Storage Life (HTSL) Conditions:
Stress Duration: 168, 500, 1000, 1500 hours.
Temperature: 150°C
Method: Lattice Document # 87-101925 and JESD22-A103 / JESD22-A117

Table 3.2.2: High Temperature Storage Life Results

Product Name	Assembler	Package	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	1500 Hrs Result	Cumulative Hours
LA4064V	ASEM	100 TQFP	Lot #1	78	0	0	0		78000
LA4064V	ASEM	100 TQFP	Lot #2	77	0	0	0		77000
LA4064V	ASEM	100 TQFP	Lot #3	78	0	0	0		78000
LA4064V	Amkor	100 TQFP	Lot #2	79	0	0	0	0	118500
GAL22V10D	UNISEM	32 QFN	Lot #1	77			0		77000
GAL22V10D	UNISEM	32 QFN	Lot #2	77			0		77000
GAL22V10D	UNISEM	32 QFN	Lot #3	77			0		77000

Cumulative HTSL Failure Rate = 0 / 543
Cumulative HTSL Device Hours = 582,500

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3.3 ispCLOCK Product Family – ESD and Latch UP Data

Electrostatic Discharge-Human Body Model:

ispCLOCK product family was tested per the JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure and Lattice Procedure # 70-100844.
All units were tested at 25^{0}C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.3.1 ispCLOCK ESD-HBM Data

Device Type	48-QFN	64-QFN	48-TQFP	64-TQFP	100-TQFP
ispPAC-CLK5620A					>2000V Class 2
ispPAC-CLK5610A			>2000V Class 2		
ispPAC-CLK5410D		>2000V Class 2			
ispPAC-CLK5406D	>2000V Class 2				
ispPAC-CLK5320S				>2000V Class 2	
ispPAC-CLK5316S				>2000V Class 2	
ispPAC-CLK5312S			>2000V Class 2		
ispPAC-CLK5308S			>2000V Class 2		
ispPAC-CLK5304S			>2000V Class 2		

HBM classification for Commercial/Industrial products, per JESD22-A114

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Electrostatic Discharge-Charged Device Model:

ispCLOCK product family was tested per the JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure and Lattice Procedure # 70-100844.

All units were tested at 25^0C prior to reliability stress and after reliability stress. No failures were observed within the passing Classification.

Table 3.3.2 ispCLOCK ESD-CDM Data

Device Type	48-QFN	64-QFN	48-TQFP	64-TQFP	100-TQFP
ispPAC-CLK5620A					>1000V Class IV
ispPAC-CLK5610A			>1000V Class IV		
ispPAC-CLK5410D		>1000V Class IV			
ispPAC-CLK5406D	>1000V Class IV				
ispPAC-CLK5320S				>1000V Class IV	
ispPAC-CLK5316S				>1000V Class IV	
ispPAC-CLK5312S			>1000V Class IV		
ispPAC-CLK5308S			>1000V Class IV		
ispPAC-CLK5304S			>1000V Class IV		

CDM classification for Commercial/Industrial products, per JESD22-C101

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Latch-Up:

ispCLOCK product family devices were tested per the JEDEC EIA/JESD78 IC Latch-up Test procedure and Lattice Procedure # 70-101570.

All units were tested at 25^0C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Earlier latch-up testing at Lattice was hardware limited to room temperature testing. Additionally, maximum-rated ambient temperature latch-up testing is generally considered to be approximately 2X worse than the trigger values found at room temperature. In order to guard band our room temperature IO latch-up testing the standard was 4X, or +/- 400mA trigger current. Therefore, the previous Lattice I/O LU standard was >400mA at room temperature, while the present standard is >100mA at maximum-rated ambient temperature.

Table 3.3.3 ispCLOCK I/O Latch Up Data

Device Type	48-QFN	64-QFN	48-TQFP	64-TQFP	100-TQFP
ispPAC-CLK5620A					>+/- 400mA Using the old Lattice standard at room temp
ispPAC-CLK5610A			>+/- 400mA Using the old Lattice standard at room temp		
ispPAC-CLK5410D		>+/- 100mA Class II, Level A			
ispPAC-CLK5406D	>+/- 100mA Class II, Level A				
ispPAC-CLK5320S				>+/- 400mA Using the old Lattice standard at room temp	
ispPAC-CLK5316S				>+/- 400mA Using the old Lattice standard at room temp	
ispPAC-CLK5312S			>+/- 400mA Using the old Lattice standard at room temp		
ispPAC-CLK5308S			>+/- 400mA Using the old Lattice standard at room temp		
ispPAC-CLK5304S			>+/- 400mA Using the old Lattice standard at room temp		

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Table 3.3.4 ispCLOCK Vcc Latch Up Data

Device Type	48-QFN	64-QFN	48-TQFP	64-TQFP	100-TQFP
ispPAC-CLK5620A					>1.5*Vcc Class II
ispPAC-CLK5610A			>1.5*Vcc Class II		
ispPAC-CLK5410D		>1.5*Vcc Class II			
ispPAC-CLK5406D	>1.5*Vcc Class II				
ispPAC-CLK5320S				>1.5*Vcc Class II	
ispPAC-CLK5316S				>1.5*Vcc Class II	
ispPAC-CLK5312S			>1.5*Vcc Class II		
ispPAC-CLK5308S			>1.5*Vcc Class II		
ispPAC-CLK5304S			>1.5*Vcc Class II		

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4.0 PACKAGE QUALIFICATION DATA FOR ispCLOCK PRODUCT FAMILY

The ispCLOCK product family is offered in TQFP and QFNs packages. To cover the range of die in the largest package types for this product family, different package and die combinations were chosen as the generic qualification vehicles for all the package qualification tests including, Temperature Cycling (T/C), Un-biased HAST (UHAST)and Biased HAST (BHAST). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection.

The generation and use of generic data is applied across a family of products or packages emanating from one base wafer foundry or assembly process is a Family Qualification, or Qualification by Extension. For the package stresses BHAST and UHAST, these are considered generic for a given Package Technology. T/C is considered generic up to an evaluated die size + package size + 10%, for a given Package Technology. Surface Mount Pre-Conditioning (SMPC) is considered generic up to an evaluated Peak Reflow temperature, for a given Package Technology. The following table demonstrates the package qualification matrix.

Table 4.1 ispCLOCK Product-Package Qualification-By-Extension Matrix

		ATK / Unisem		ASEM / ATK / Unisem		
Product / Package	**Stress Test**	**48-QFN**	**64-QFN**	**48-TQFP**	**64-TQFP**	**100-TQFP**
ispPAC-CLK5620A	SMPC	Packages not offered		Packages not offered		MSL3
	Temp Cycle					1000 cycles
	BHAST / 8585					(2) Qual by Ext
	UHAST					(2) Qual by Ext
	(1) HTSL					1000 hours
ispPAC-CLK5610A	SMPC	Packages not offered		(3) Qual by Ext	Packages not offered	
	Temp Cycle			(3) Qual by Ext		
	BHAST / 8585			(2) Qual by Ext		
	UHAST			(2) Qual by Ext		
	HTSL			(3) Qual by Ext		
ispPAC-CLK5410D	SMPC	Package not offered	MSL3	Packages not offered		
	Temp Cycle		1000 cycles			
	BHAST / 8585		(4) Qual by Ext			
	UHAST		(4) Qual by Ext			
	HTSL		1000 hours			
ispPAC-CLK5406D	SMPC	(5) Qual by Ext	Package not offered	Packages not offered		
	Temp Cycle	(5) Qual by Ext				
	BHAST / 8585	(5) Qual by Ext				
	UHAST	(5) Qual by Ext				
	HTSL	(5) Qual by Ext				
ispPAC-CLK5320S	SMPC	Packages not offered		Package not offered	MSL3	Package not offered
	Temp Cycle				1000 cycles	
	BHAST / 8585				(2) Qual by Ext	
	UHAST				(2) Qual by Ext	
	HTSL				(3) Qual by Ext	
ispPAC-CLK5316S	SMPC	Packages not offered		Package not offered	(3) Qual by Ext	Package not offered
	Temp Cycle				(3) Qual by Ext	
	BHAST / 8585				(2) Qual by Ext	
	UHAST				(2) Qual by Ext	
	HTSL				(3) Qual by Ext	
ispPAC-CLK5312S	SMPC	Packages not offered		MSL3	Packages not offered	
	Temp Cycle			1000 cycles		
	BHAST / 8585			(2) Qual by Ext		
	UHAST			(2) Qual by Ext		
	HTSL			(3) Qual by Ext		
ispPAC-CLK5308S	SMPC	Packages not offered		(3) Qual by Ext	Packages not offered	
	Temp Cycle			(3) Qual by Ext		
	BHAST / 8585			(2) Qual by Ext		
	UHAST			(2) Qual by Ext		
	HTSL			(3) Qual by Ext		
ispPAC-CLK5304S	SMPC	Packages not offered		(3) Qual by Ext	Packages not offered	
	Temp Cycle			(3) Qual by Ext		
	BHAST / 8585			(2) Qual by Ext		
	UHAST			(2) Qual by Ext		
	HTSL			(3) Qual by Ext		

Note: (1) HTSL run as HTRX. The same 150C bake stress conditions.
(2) Qualified by extension from ispMACH4128, 144-TQFP.
(3) Qualified by extension from ispCLK5620A, 100-TQFP.
(4) Qualified by extension from GAL22V10D, QFN.
(5) Qualified by extension from CLK5410D, QFN.

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4.1 ispCLOCK Product Family Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JEDEC JESD22-A113 "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3(MSL3) package moisture sensitivity and dry-pack storage requirements.

Surface Mount Preconditioning (MSL3)
(10 Temperature Cycles between -55°C and 125°C, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, 225/245/250/260 °C Reflow Simulation, 3 passes) performed before all package tests.
MSL3 Packages: TQFP, QFNs
Method: Lattice Procedure # 70-103467, J-STD-020 and JESD22-A113

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
ispPAC-CLK5312	48 TQFP	Amkor	Lot #1	45	0	260°C
ispPAC-CLK5312	48 TQFP	Amkor	Lot #2	45	0	260°C
ispPAC-CLK5320	64 TQFP	Amkor	Lot #1	45	0	260°C
ispPAC-CLK5320	64 TQFP	Amkor	Lot #2	45	0	260°C
ispPAC-CLK5520	100 TQFP	Amkor	Lot #1	47	0	260°C
ispPAC-CLK5520	100 TQFP	Amkor	Lot #2	47	0	260°C
ispPAC-CLK5410D	64 QFN	Amkor	Lot #1	75	0	260°C
ispPAC-CLK5410D	64 QFN	Amkor	Lot #2	72	0	260°C
GAL22V10D	32 QFN	Unisem	Lot #1	154	0	260°C
GAL22V10D	32 QFN	Unisem	Lot #2	154	0	260°C
GAL22V10D	32 QFN	Unisem	Lot #3	154	0	260°C
POWR6AT6	32 QFN	Unisem	Lot #4	77	0	260°C
POWR6AT6	32 QFN	Unisem	Lot #5	77	0	260°C
ispPAC-POWR1208	44 TQFP	Unisem	Lot #1	77	0	260°C
ispPAC-POWR1208	44 TQFP	Unisem	Lot #1	77	0	260°C
ispPAC-POWR1208	44 TQFP	Unisem	Lot #1	77	0	260°C
ispMACH 4512	176TQFP	Unisem	Lot#3	75	0	260°C
ispMACH 4512	176TQFP	Unisem	Lot#1	99	0	260°C
ispMACH 4512	176TQFP	Unisem	Lot#2	98	0	260°C
LA4128V	144 TQFP	ASEM	Lot #1	234	0	260°C
LA4128V	144 TQFP	ASEM	Lot #2	231	0	260°C
LA4128V	144 TQFP	ASEM	Lot #3	234	0	260°C
LA4128V	144 TQFP	Amkor	Lot #1	81	0	260°C
LA4128V	144 TQFP	Amkor	Lot #2	82	0	260°C
LA4128V	144 TQFP	Amkor	Lot #3	78	0	260°C
LA4128V	144 TQFP	Amkor	Lot #4	162	0	260°C
LA4128V	144 TQFP	Amkor	Lot #5	200	0	260°C
LA4128V	144 TQFP	Amkor	Lot #6	200	0	260°C

Cumulative SMPC Failure Rate = 0 / 3,042

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4.2 – ispCLOCK Product Family Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104 "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, QFN
Stress Duration: 1000 cycles
Stress Conditions: Temperature cycling between -55°C to 125°C
Method: Lattice Procedure # 70-101568 and JESD22-A104

Table 4.2.1: Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Quantity	250 Cycles	500 Cycles	1000 Cycles
ispPAC-CLK5312	48 TQFP	Amkor	Lot #1	45	0	0	0
ispPAC-CLK5312	48 TQFP	Amkor	Lot #2	45	0	0	0
ispPAC-CLK5320	64 TQFP	Amkor	Lot #1	45	0	0	0
ispPAC-CLK5320	64 TQFP	Amkor	Lot #2	45	0	0	0
ispPAC-CLK5520	100 TQFP	Amkor	Lot #1	47	0	0	0
ispPAC-CLK5520	100 TQFP	Amkor	Lot #2	47	0	0	0
ispPAC-CLK5410D	64 QFN	Amkor	Lot #1	75	0	0	0
ispPAC-CLK5410D	64 QFN	Amkor	Lot #2	72	0	0	0
POWR6AT6	32 QFN	Unisem	Lot #4	77	0	0	0
POWR6AT6	32 QFN	Unisem	Lot #5	77	0	0	0
ispPAC-POWR1208	44 TQFP	Unisem	Lot #1	77	0	0	0
ispPAC-POWR1208	44 TQFP	Unisem	Lot #1	77	0	0	0
ispPAC-POWR1208	44 TQFP	Unisem	Lot #1	77	0	0	0
ispMACH 4512	176TQFP	Unisem	Lot#1	50	0	0	0
ispMACH 4512	176TQFP	Unisem	Lot#2	49	0	0	0
ispMACH 4512	176TQFP	Unisem	Lot#3	45	0	0	0
LA4128V	144 TQFP	ASEM	Lot #1	77	0	0	0
LA4128V	144 TQFP	ASEM	Lot #2	77	0	0	0
LA4128V	144 TQFP	ASEM	Lot #3	77	0	0	0
LA4128V	144 TQFP	Amkor	Lot #1	81	0	0	0
LA4128V	144 TQFP	Amkor	Lot #2	82	0	0	0
LA4128V	144 TQFP	Amkor	Lot #3	78	0	0	0

Cumulative Temp Cycle Failure Rate = 0 / 1,422

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4.3 Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent JEDEC JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," the Unbiased HAST conditions are 96 hour exposure at 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, QFN
Stress Duration: 96 Hrs
Stress Conditions: 130°C, 15psig, 85% RH
Method: Lattice Procedure # 70-104285 and JESD22-A118

Table 4.3.1: Unbiased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
GAL22V10D	32 QFN	Unisem	Lot #1	77	0	96 Hrs
GAL22V10D	32 QFN	Unisem	Lot #2	77	0	96 Hrs
GAL22V10D	32 QFN	Unisem	Lot #3	77	0	96 Hrs
ispMACH 4512	176TQFP	Unisem	Lot#1	49	0	96 Hrs
ispMACH 4512	176TQFP	Unisem	Lot#2	49	0	96 Hrs
ispMACH 4512	176TQFP	Unisem	Lot#3	30	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #1	77	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #2	75	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #3	77	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #4	81	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #5	100	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #6	100	0	96 Hrs

Cumulative Unbiased HAST failure Rate = 0 / 869

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4.4 THB: Biased HAST Data

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD A110-B "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are with Vcc bias and alternate pin biasing in an ambient of 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, QFN
Stress Conditions: Vcc= 1.95V/ 3.6V, 130°C / 85% RH, 15 psig
Stress Duration: 96 hours
Method: Lattice Procedure # 70-101571 and JESD22-A101

Table 4.4.1: Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
GAL22V10D	32 QFN	Unisem	Lot #1	77	0	96 Hrs
GAL22V10D	32 QFN	Unisem	Lot #2	77	0	96 Hrs
GAL22V10D	32 QFN	Unisem	Lot #3	77	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #1	80	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #2	77	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #3	80	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #4	81	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #5	100	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #6	100	0	96 Hrs

Cumulative BHAST failure Rate = 0 / 749

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5.0 ispCLOCK Process Reliability Wafer Level Review

Several key fabrication process related parameters have been identified by the foundry that would affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. Normal operating conditions are defined in the Electrical Design Rules (EDR). These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence. SM is not an issue for the UM10 BEOL (etched Al lines, W plug Vias, SiO IMD).

Table 5.1 – Wafer Level Reliability Results for UM10 (0.22um) Process Technology

HCI

Device	ne	pe	ns	nx	nt
Tox	55A	55A	90A	90A	210A
delta Ids	-10%	-10%	-10%	-10%	-10%
Celsius	25	25	25	25	25
Vgstress	Vd/2	0	Vd/2	Vd/2	Vd/2
Vds	2.75	-2.75	2.75	3.6	3.6
TTF	5 lots>12yr	1 lot 43yr	1 lot 1.4Myr	1 lot 65yr	1 lot 11500yr

TDDB

Device	ne	pe	ns	nx	px	nt	pt
Celsius	130	130	130	130	130	130	130
Vg	2.75	-2.75	3.6	3.6	-3.6	4.8	-4.8
Area	72900um^2	72900um^2	72900um^2	72900um^2	72900um^2	72900um^2	4374um^2
0.1% TTF	2 lots>134yr	1 lot 534yr	1 lot 3000yr	1 lot 4000yr	1 lot 4500yr	1 lot 6200yr	1 lot 650kyr

EML

Layer	M1	M2	M3	M4	M5
Celsius	130	130	130	130	130
delta R	20%	20%	20%	20%	20%
Jmax	1.78mA/um^2	1.78mA/um^2	1.78mA/um^2	1.78mA/um^2	2.08mA/um^2
0.1%TTF	4 lots>22yr	4 lots>62yr	3 lots>40yr	3 lots>17yr	54 lots>11yr

Note: Reliability life times are based on listed temperature and used conditions. Detailed WLR test conditions are available upon request.

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6.0 ispCLOCK PACKAGE ASSEMBLY INTEGRITY TESTS

6.1 Wire Bond Shear Test

This procedure is used to measure the wire bond strength at the ball joints. Thirty bonds from a minimum of five devices were used for Wire Bond Shear.

WIRE BOND SHEAR TEST RESULTS: All bond shear observations were > 15 grams for TQFP packages tested.

The average measured bond shear results for TQFP were Cpk of > 3.7 and Ppk of > 3.7.

6.2 Wire Bond Pull

This procedure is used to measure the wire bond strength at the ball joints and stitch bonds.
For products evaluation thirty bonds from a minimum of five devices were used for and Wire Bond Pull. Test conditions for these tests were 6 grams minimum for 1.0 mil gold wire

WIRE BOND PULL RESULTS: All bond pull observations were >6 grams for TQFP packages tested.

The average measured wire bond pull results for TQFP were Cpk of > 2.0 and Ppk of > 2.1.

6.3 Solderability

This procedure is used to evaluate the solderability of device terminals normally joined by a soldering operation. An accelerated aging test is included in this test method, which simulates natural aging under a combination of various storage conditions that have deleterious effects. Units are exposed to a 8 hour steam preconditioning followed a flux exposure for 7 seconds and a dip in Pb-free solder alloy @ 245 °C ± 5°C for 5 seconds. Minimum of 22 leads from 3 devices per lot were tested with zero failure acceptance.

No failures were observed for TQFP packages. All the tested units passed. There was less than 5% pitting and dewetting on the solder covered area.

No failures were observed for QFN packages. All the tested units passed. There was less than 5% pitting and dewetting on the solder covered area.

6.4 Physical Dimensions

Devices were measured using the appropriate Lattice Semiconductor case outline drawings.

The 10 devices of TQFP from 3 different lots were measured with no failures found. The calculated Cpk on this small sample is Cpk > 9.6.

Note: ispCLOCK TQFP and QFN packages are qualified by extension from ispMACH 4000 and ispPAC-POWR devices.

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7.0 ispCLOCK ADDITIONAL FAMILY DATA

Table 7.1: ispCLOCK Package Assembly Data- TQFP / QFN

Package Attributes / Assembly Sites	ASEM	Amkor	UNISEM
Die Family (Product Line)	ispCLOCK	ispCLOCK	ispCLOCK
Fabrication Process Technology	UM10 (0.22um CMOS)	UM10 (0.22um CMOS)	UM10 (0.22um CMOS)
Package Assembly Site	Malaysia	Korea	Indonesia
Package Type	TQFP/ QFN	TQFP / QFN	TQFP / QFN
Pin Count	48/ 64/ 100 48/ 64	48/ 64/100 48/ 64	48/ 64/100 48/ 64
Die Preparation/Singulation	wafer saw, full cut	wafer saw, full cut	wafer saw, full cut
Die Attach Material -TQFP	Ablebond 3230	Ablebond 3230	CRM1076NS
Die Attach Material -QFN	CRM 1066 Series	CRM 1066 Series	CRM 1066 Series
Mold Compound Supplier/ID - TQFP	Hitachi CEL9220HF Series	KTMC 5700TQ Sereis	Sumitomo G700 Series
Mold Compound Supplier/ID - QFN	Sumitomo G770 Series	Sumitomo G770 Series	Sumitomo G770 Series
Wire Bond Material	Gold (Au)	Gold (Au)	Gold (Au)
Wire Bond Methods	Thermosonic Ball	Thermosonic Ball	Thermosonic Bball
Lead frame Material	Cu Alloy	Cu Alloy	Cu Alloy
Lead Finish	Matte Sn (annealed)	Matte Sn (annealed)	Matte Sn (annealed)
Marking	Laser	Laser	Laser

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