Lattice ispMACH 4000 V/B/C/ZC/ZE Product Family Qualification Summary

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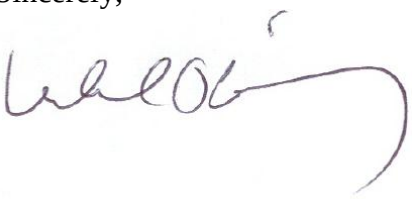
Dear Customer,

Welcome to the Lattice Semiconductor Corp. ispMACH® 4000 Product Family Qualification Report. This report reflects our continued commitment to product quality and reliability. The information in this report is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

The information contained in this document is extensive, and represents the entire qualification effort for this device family. Our goal is to provide this information to support your decision making process, and to facilitate the selection and use of our products.

As always, your feedback is valuable to Lattice. Our goal is to continuously improve our systems, including the generation of this report and the data included. Please feel free to forward your comments and suggestions to your local Lattice representative. We will use that feedback carefully and wisely in our effort to maximize customer satisfaction.

Sincerely,



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1.0 INTRODUCTION

The ispMACH 4000 Product Family offers a SuperFAST CPLD solution. The ispMACH 4000 Family includes 3.3, 2.5, 1.8 volt power supply, and 1.8- volt zero power versions, designated ispMACH 4000V, ispMACH 4000B, ispMACH 4000C, ispMACH 4000ZC and ispMACH 4000ZE devices respectively. The ispMACH 4000V/B/C/ZC/ZE Product Family offers densities ranging from 32 to 512 macrocells.

The ispMACH 4000V/B/C/ZC/ZE product families are built on Lattice Semiconductor's 3.3V/2.5V/1.8V EE9 process. EE9 is a shallow trench isolated 0.18um Leff CMOS process with Electrically Erasable cell (E2 cell) modules. This process uses five, planarized metal interconnect layers and single layer polysilicon.

The ispMACH 4000V/B/C/ZC product family was initially built at United Microelectronics Company (UMC). The Lattice ispMACH 4256 device was the initial product released to production in May 2001. The additional foundry, Seiko Epson, was released in July 2003. In 2002, Lattice Semiconductor introduced the extended temperature grade, -40 to 130°C junction (T_J), ispMACH 4000V/ ZC products (V = 3.3V, Z = zero power, 1.8 V).

This report details the reliability qualification results of the initial ispMACH 4000V/B/C/ZC/ZE product introduction built at Seiko Epson and United Microelectronics Company (UMC). To verify product reliability, Lattice Semiconductor maintains an active Early Life and Inherent Life Reliability Monitor program on the ispMACH 4000 products. Lattice Semiconductor publishes the Reliability Monitor Data quarterly.

Table 1.1 Lattice ispMACH 4000 V/B/C Product Family Attributes

	ispMACH 4032V/B/C	**ispMACH 4064V/B/C**	**ispMACH 4128V/B/C**	**ispMACH 4256V/B/C**	**ispMACH 4384V/B/C**	**ispMACH 4512V/B/C**
Macrocells	32	64	128	256	384	512
I/O + Dedicated Inputs	30+2/32+4	30+2/32+4/64+10	64+10/92+4/96+4	64+10/96+14/128+4/160+4	128+4/192+4	128+4/208+4
tPD (ns)	2.5	2.5	2.7	3.0	3.5	3.5
tS (ns)	1.8	1.8	1.8	2.0	2.0	2.0
tCO (ns)	2.2	2.2	2.7	2.7	2.7	2.7
fMAX (MHz)	400	400	333	322	322	322
Supply Voltages (V)	3.3/2.5/1.8V	3.3/2.5/1.8V	3.3/2.5/1.8V	3.3/2.5/1.8V	3.3/2.5/1.8V	3.3/2.5/1.8V
Fabrication Site	Seiko Epson / UMC Taiwan	Seiko Epson / UMC Taiwan	Seiko Epson / UMC Taiwan	Seiko Epson / UMC Taiwan	Seiko Epson / UMC Taiwan	Seiko Epson / UMC Taiwan
Process Technology	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)
Die Size (W x L x T)	1770 x 1910 x 330-381 (um)	2530 x 2330 x 330-381 (um)	3280 x 3150 x 330-381 (um)	3530 x 4180 x 330-381 (um)	5300 x 5000 x 330-381 (um)	5400 x 5500 x 330-381 (um)
Die Metallization	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu
Die Interconnect Dielectric	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS
Pins/Package	44 TQFP 48 TQFP	44 TQFP 48 TQFP 100 TQFP	100 TQFP 128 TQFP 144 TQFP[1]	100 TQFP 144 TQFP[1] 176 TQFP 256 ftBGA²/fpBGA[2, 3]	176 TQFP 256 ftBGA/fpBGA[3]	176 TQFP 256 ftBGA/fpBGA[3]

1. 3.3V (4000V) only.
2. 128-I/O and 160-I/O configurations.
3. Use 256 ftBGA package for all new designs. Refer to PCN#14A-07 for 256 fpBGA package discontinuance.

Table 1.2 Lattice ispMACH 4000ZC Product Family Attributes

	ispMACH 4032ZC	ispMACH 4064ZC	ispMACH 4064ZC	ispMACH 4256ZC
Macrocells	32	64	128	256
I/O + Dedicated Inputs	32+4/32+4	32+4/32+12/ 64+10/64+10	64+10/96+4	64+10/96+6/ 128+4
tPD (ns)	3.5	3.7	4.2	4.5
tS (ns)	2.2	2.5	2.7	2.9
tCO (ns)	3.0	3.2	3.5	3.8
fMAX (MHz)	267	250	220	200
Supply Voltages (V)	1.8	1.8	1.8	1.8
Max, Standby Icc (µA)	20	25	35	55
Fabrication Site	Seiko Epson / UMC Taiwan	Seiko Epson / UMC Taiwan	Seiko Epson / UMC Taiwan	Seiko Epson / UMC Taiwan
Process Technology	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)
Die Size **(W x L x T)**	1770 x 1910 x 330-381 (um)	2490 x 1960 x 330-381 (um)	2490 x 1960 x 330-381 (um)	3530 x 4180 x 330-381 (um)
Die Metallization	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu
Die Interconnect Dielectric	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS
Pins/Package	48 TQFP 56 csBGA	48 TQFP 56 csBGA 100 TQFP 132 csBGA	100 TQFP 132 csBGA	100 TQFP 132 csBGA 176 TQFP

Table 1.3 Lattice ispMACH 4000ZE Product Family Attributes

	ispMACH 4032ZE	ispMACH 4064ZE	ispMACH 4128ZE	ispMACH 4256ZE
Macrocells	32	64	128	256
I/O + Dedicated Inputs	32+4/32+4	32+4/48+4/48+4 64+10/64+10	64+10/96+4/96+4/ 96+4	64+10/96+14/ 108+4
tPD (ns)	4.4	4.7	5.8	5.8
tS (ns)	2.2	2.5	2.9	2.9
tCO (ns)	3.0	3.2	3.8	3.8
fMAX (MHz)	260	241	200	200
Supply Voltages (V)	1.8V	1.8V	1.8V	1.8V
Fabrication Site	Seiko Epson / UMC Taiwan	Seiko Epson / UMC Taiwan	Seiko Epson	Seiko Epson
Process Technology	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)
Die Size **(W x L x T)**	1770 x 1910 x 330-381 (um)	2490 x 1960 x 330-381 (um)	3280 x 3150 x 330-381 (um)	3530 x 4180 x 330-381 (um)
Die Metallization	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu
Die Interconnect Dielectric	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS
Pins/Packages **(Lead-Free only)**	48 TQFP 64 csBGA	48 TQFP 64 csBGA 64 ucBGA 100 TQFP 144 csBGA	100 TQFP 132 ucBGA 144 TQFP 144 csBGA	100 TQFP 144 TQFP 144 csBGA

Lattice offers automotive version of ispMACH 4000 family. This high performance LA-ispMACH 4000V automotive family offers a SuperFAST 3.3 volt CPLD solution that is tested and qualified to the AEC-Q100 standard.

The LA-ispMACH 4000ZC automotive family combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The LA-ispMACH 4000V automotive family offers densities ranging from 32 to 128 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP) packages ranging from 44 to 144 pins. Table 1.4 shows the macrocell, package and I/O options, along with other key parameters.

Table 1.4 Lattice Automotive LA-ispMACH 4000V Product Family Attributes

	LA-ispMACH 4032V	**LA-ispMACH 4064V**	**LA-ispMACH 4128V**
Macrocells	32	64	128
I/O + Dedicated Inputs	30+2/32+4	30+2/32+4/64+10	64+10/92+4/96+4
tPD (ns)	7.5	7.5	7.5
tS (ns)	4.5	4.5	4.5
tCO (ns)	4.5	4.5	4.5
fMAX (MHz)	168	168	168
Supply Voltage (V)	3.3V	3.3V	3.3V
Fabrication Site	Seiko Epson	Seiko Epson	Seiko Epson
Process Technology	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)
Die Size (W x L x T)	1770 x 1910 x 330-381 (um)	2490 x 1960 x 330-381 (um)	3280 x 3150 x 330-381 (um)
Die Metallization	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu
Die Interconnect Dielectric	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS
Pins/Package (Lead-Free Only)	44 TQFP 48 TQFP	44 TQFP 48 TQFP 100 TQFP	100 TQFP 128 TQFP 144 TQFP

The LA-ispMACH 4000V automotive family has enhanced system integration capabilities. It supports 3.3V supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The LA-ispMACH 4000V also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The LA-ispMACH 4000V automotive family is in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment.

The LA-ispMACH 4000ZC automotive family shares most of the same traits as the LA-ispMACH4000V family. The exception is that the Supply Voltage is 1.8V which categorizes this part as Low-Power. The LA-ispMACH 4000ZC automotive family offers densities ranging from 32 to 128 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP) packages ranging from 44 to 144 pins. Table 1.5 shows the macrocell, package and I/O options, along with other key parameters.

Table 1.5 Lattice Automotive LA-ispMACH 4000ZC Product Family Attributes

	LA-ispMACH 4032ZC	LA-ispMACH 4064ZC	LA-ispMACH 4128ZC
Macrocells	32	64	128
I/O + Dedicated Inputs	32+4	32+4/64+10	64+10
tPD (ns)	7.5	7.5	7.5
tS (ns)	4.5	4.5	4.5
tCO (ns)	4.5	4.5	4.5
fMAX (MHz)	168	168	168
Supply Voltage (V)	1.8V	1.8V	1.8V
Fabrication Site	Seiko Epson	Seiko Epson	Seiko Epson
Process Technology	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)	EE9 180nm (E2 cell)
Die Size (W x L x T)	1770 x 1910 x 330-381 (um)	2490 x 1960 x 330-381 (um)	3280 x 3150 x 330-381 (um)
Die Metallization	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu
Die Interconnect Dielectric	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS
Pins/Package (Lead-Free Only)	48 TQFP	48 TQFP 100 TQFP	100 TQFP

The LA-ispMACH 4000V/ZC automotive family is built on the 0.18 um EE9 Electrically Erasable (E2 cell based) CMOS process at Seiko Epson and assembled at Amkor Technology, Korea and Advance Semiconductor Engineering, Malaysia (ASEM) in Pb-free TQFP packages. This report includes the automotive reliability qualification and device characterization results of the initial Lattice Automotive LA4000V/ZC Product Family introduction.

This report summarizes the qualification results for all Lattice ispMACH 4000V/B/C/ZC/ZE and LA-ispMACH4000V/ZC products as ofJuly 2011.

2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8 Discipline (8D) process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

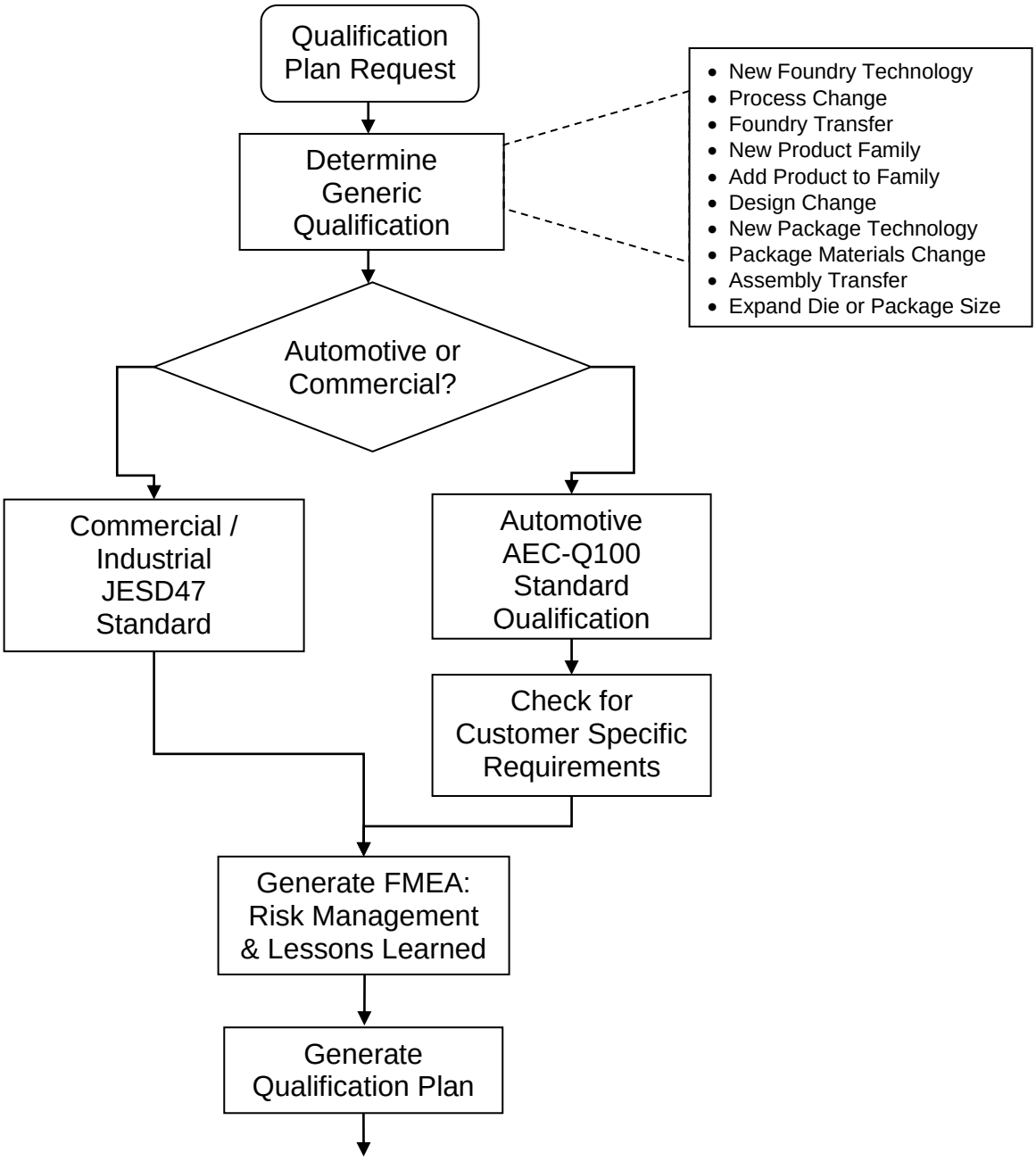
Failure rates in this reliability report are expressed in FITS. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Tables 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The ispMACH 4000V/B/C/ZC/ZE and LA-ispMACH 4000V/ZC product families are built on Lattice Semiconductor's 1.8V/2.5V/3.3V EE9 process. EE9 is a shallow trench isolated 0.18um Leff CMOS process with Electrically Erasable cell (E^2 cell) modules. This process uses five, planarized metal interconnect layers and single layer polysilicon.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at www.latticesemi.com/lit/docs/qa/product_reliability_monitor.pdf .

Figure 2.1: ispMACH 4000 Product Qualification Process Flow



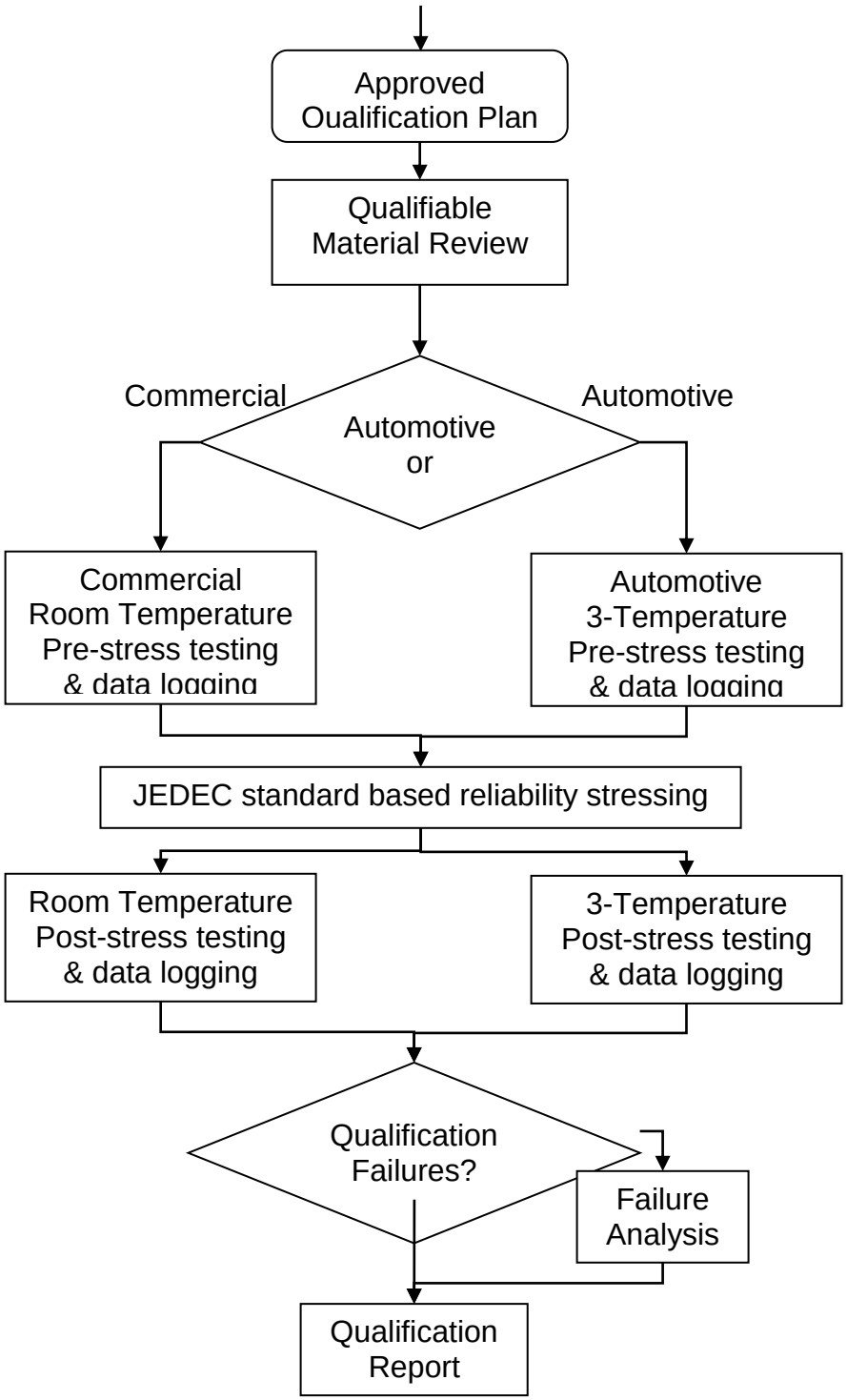

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Table 2.2: Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 87-101943, MIL-STD-883, Method 1005.8, JESD22-A10 ispMACH-4000 LA-ispMACH-4000	125° C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs. Preconditioned with 100 read/write cycles	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
High Temp Data Retention HTRX	Lattice Procedure # 87-101925, JESD22-A117 ispMACH-4000 LA-ispMACH-4000	150° C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs. Preconditioned with 100 read/write cycles	100/lot 2-3 lots	Design, Foundry Process, Package Qualification E^2 Cell Products Flash based Products
High Temp Storage Life HTSL	Lattice Procedure # 87-101925, JESD22-A103 ispMACH-4000 LA-ispMACH-4000	150° C, at 168, 500, 1000, 2000 hours.	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
Endurance - Program/Erase Cycling Flash based Products	Lattice Procedure, # 70-104633 JESD22-A117 ispMACH-4000 LA-ispMACH-4000	Program/Erase devices to 10,000 cycles Program/Erase devices to 10X cycles of data sheet specification	10/lot 2-3 lots typical	Design, Foundry Process, Package Qualification
ESD HBM	Lattice Procedure # 70-100844, MIL-STD-883, Method 3015.7 JESD22-A114	Human Body Model (HBM) sweep to 2000 volts – (130nm and older)	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD CDM	Lattice Procedure # 70-100844, JESD22-C101	Charged Device model (CDM) sweep to 1000 volts (130nm and older)	3 parts/lot 1-3 lots typical	Design, Foundry Process
Latch Up Resistance LU	Lattice Procedure # 70-101570, JESD78	±100 ma on I/O's, Vcc +50% on Power Supplies. (Max operating temp.)	6 parts/lot 1-3 lots typical	Design, Foundry Process
Surface Mount Pre-conditioning SMPC	Lattice Procedure # 70-103467, IPC/JEDEC J-STD-020D.1 JESD-A113 CPLD/FPGA - MSL 3	10 Temp cycles, 24 hr 125° C Bake 192hr. 30/60 Soak 3 SMT simulation cycles	All units going into Temp Cycling, UHAST, BHAST, 85/85	Plastic Packages only
Temperature Cycling TC	Lattice Procedure #70-101568, MIL-STD- 883, Method 1010, Condition B JESD22-A104	(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment	45 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification
Unbiased HAST UHAST	Lattice Procedure # 70-104285 JESD22-A118	96 hrs, 130 C, or 264 hrs 110 C, and 85% Relative Humidity	45 parts/lot 2-3 lots	Foundry Process, Package Qualification Plastic Packages only

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
Moisture Resistance Temperature Humidity Bias 85/85 THBS or Biased HAST BHAST	Lattice Procedure # 70-101571, JESD22-A101 JESD22-A110	Biased to maximum operating Vcc, 85° C, 85% Relative Humidity, 1000 hours or Biased to maximum operating Vcc, 96 hrs, 130 C, 85% Relative Humidity or Biased to maximum operating Vcc, 264 hrs 110 C, and 85% Relative Humidity	45 devices/lot 2-3 lots	Design, Foundry Process, Package Qualification Plastic Packages only
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or applicable LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	Package Qualification
Wire Bond Strength	Lattice Procedure # 70-100220	Per package type	15 devices per pkg. per year	Design, Foundry Process, Package Qualification
Solderability	Lattice Procedure # 70-100212, MIL-STD-883, Method 2003	Steam Pre-conditioning 4-8 hours. Solder dip at 245°C+5°C	22 leads/ 3 devices/ Package family	All packages except BGAs

3.0 QUALIFICATION DATA FOR EE9 PROCESS TECHNOLOGY

The ispMACH 4000V/B/C/ZC/ZE product family is built on Lattice Semiconductor's EE9 180nm E^2CMOS process technology. The ispMACH 4000V/B/C/ZC product family was initially built at United Microelectronics Company (UMC). The Lattice ispMACH 4256 device was the initial product released to production in May 2001. The additional foundry, Seiko Epson, was released in July 2003.

The LA-ispMACH 4000V/ZC automotive family was qualified for automotive applications using the Stress Test Qualification for Integrated Circuits, AEC-Q100-Rev-F, test requirements and methods. The LA-ispMACH 4000V/ZC automotive family operates over the Automotive Grade 1 (-40^0C to $+125^0$C) ambient operation temperature range. All low and high temperature test read-outs were performed at the Grade 1 temperature extremes.

Product Family: ispMACH 4000V/B/C/ZC/ZE, LA-ispMACH 4000V/ZC
Packages offered: csBGA, ftBGA, fpBGA, ucBGA and TQFP
Process Technology Node: 180nm

3.1 EE9 Product Family Life Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

EE9 Life Test (HTOL) Conditions:

Stress Duration: 48, 168, 500, 1000, 2000 hours.
Temperature: 125°C
Stress Voltage ispMACH 4000V/B/C/ZC/ZE: V_{CC}=1.95V
Stress Voltage LA-ispMACH 4000V: V_{CC}=3.6V/ V_{CCIO}=3.6V
Stress Voltage LA-ispMACH 4000ZC: V_{CC}=2.0V / V_{CCIO}=3.6V
Preconditioned with 1000 read/write cycles
Method: Lattice Document # 87-101943 and JESD22-A108C

Table 3.1.1: EE9 Product Family HTOL Results

Product Name	Foundry	Lot #	Qty	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
LC4032ZC	Seiko	Lot #1	77		0	0	0	0	154,000
LC4032ZC	Seiko	Lot #2	77		0	0	0	0	154,000
LC4032ZE	Seiko	Lot #1	77		0	0	0		77,000
LC4032ZE	Seiko	Lot #2	77		0	0	0		77,000
LC4064ZC	Seiko	Lot #1	77		0	0	0		77,000
LC4064ZC	Seiko	Lot #2	77		0	0	0		77,000
LC4064ZE	Seiko	Lot #1	77		1[A]	0	0		76,000*
LC4064ZE	Seiko	Lot #2	77		0	1[B]	0		76,000*
LC4128	Seiko	Lot #1	77		0	0	0	0	154,000
LC4128	Seiko	Lot #2	77		0	0	0	0	154,000
LC4256	Seiko	Lot #1	77		0	0	0	0	154,000
LC4256	Seiko	Lot #2	64		0	0	0	0	128,000
LC4256	Seiko	Lot #3	129		0	0	0	0	258,000
LC4256	Seiko	Lot #4	120		0	0	0	0	240,000
LC4256	Seiko	Lot #5	120		0	0	0	0	240,000
LC4032	UMC	Lot#1	77		0	0	0	0	154,000
LC4032ZC	UMC	Lot#1	77		0	0	0	0	154,000
LC4064	UMC	Lot#1	77		0	0	0	0	154,000
LC4064	UMC	Lot#2	77		0	0	0	0	154,000
LC4128	UMC	Lot#1	77		0	0	0	0	154,000
LC4256	UMC	Lot#1	174		0	0	0		174,000
LC4256	UMC	Lot#2A	169		1[C]				
LC4256	UMC	Lot#2B	186		0	0	0	0	372,000

Product Name	Foundry	Lot #	Qty	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
LC4256	UMC	Lot#2C	179		0	0	0		179,000
LC4256	UMC	Lot#3	173		0				
LC4256	UMC	Lot#4	83		0	0	0	0	166,000
LC4256	UMC	Lot#5	90		0	0	0	0	180,000
LC4256	UMC	Lot#6	90		0	0	0		90,000
LC4384	UMC	Lot#1	77		0	0	0	0	154,000
LC4512	UMC	Lot#1	77		0	0	0	0	154,000
LC4512	UMC	Lot#2	77		0	0	0	0	154,000
LA4064V	Seiko	Lot#1	77		0	0	0		77,000
LA4064V	Seiko	Lot#2	77		0	0	0		77,000
LA4064V	Seiko	Lot#3	78		0	0	0		77,000
LA4064V	Seiko	Lot#1	80		0	0	0		80,000
LA4064V	Seiko	Lot#2	80		0	0	0		80,000
LA4064V	Seiko	Lot#3	79		0	0	0		79,000
LA4064ZC	Seiko	Lot#4	128		0	0	0		128,000
LA4064ZC	Seiko	Lot#5	130		0	0	0		130,000
LA4032ZC	Seiko	Lot#1	793	0					
LA4032ZC	Seiko	Lot#2	799	0					
LA4032ZC	Seiko	Lot#3	802	0					
LA4032V	Seiko	Lot#1	798	0					
LA4032V	Seiko	Lot#2	800	0					
LA4032V	Seiko	Lot#3	798	0					
LC4032ZE	UMC	Lot#1	800	0					
LC4032ZE	UMC	Lot#2	744	0					
LC4064ZE	UMC	Lot#3	730	0					

A: 1* unit failed for EOS. FAR#1376

B: 1* unit failed for EOS. FAR#1376

* EOS units discounted from cumulative hours.

C: 1 unit failed ELFR. Root cause unknown.

FIT Rate Assumptions:
Tjstress=125C, Tjref=55C, Activation Energy = 0.5eV

EE9 Cumulative HTOL Device Hours = 5,613,360
EE9 Cumulative HTOL Sample Size = 1 / 3,426
EE9 FIT Rate = 16 FIT

EE9 Seiko Cumulative HTOL Device Hours = 3,053,920
EE9 Seiko HTOL Sample Size = 0 / 2,008
EE9 Seiko FIT Rate = 13 FIT

EE9 UMC Cumulative HTOL Device Hours = 2,559,440
EE9 UMC HTOL Sample Size = 1 / 1,418
EE9 UMC FIT Rate = 35 FIT

EE9 ELFR (48 or 168 Hrs) Cumulative Results = 1 / 10,833
EE9 UMC ELFR (48 or 168 Hrs) Results = 1 / 4,034
EE9 Seiko ELFR (48 or 168 Hrs) Results = 0 / 6,838

Low Temperature Operating Life (LTOL) Test

The Low Temperature Operating Life test is used to accelerate gain onto the floating gate due to hot electron effects. A pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at 1.95V and -55°C.

EE9 Life Test (LTOL) Conditions:

Stress Duration: 168, 500, 1000 hours.
Temperature: -55°C
Stress Voltage ispMACH 4000: V_{CC}=1.95V
Preconditioned with 1000 read/write cycles
Method: Lattice Document # 87-101943 and JESD22-A108C

Table 3.1.2: EE9 Product Family LTOL Results

Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LC4256	UMC	Lot #2	45	0	0	0	45000

EE9 Cumulative LTOL Failure Rate = 0 / 45
EE9 Cumulative LTOL Device Hours = 45,000

3.2 ispMACH 4000 Product Family High Temperature Data Retention (HTRX)

High Temperature Data Retention (HTRX)

The High Temperature Data Retention test measures the Electrically Erasable cell (E^2 cell) reliability while the High Temperature Operating Life test is structured to measure functional operating circuitry failure mechanisms. The High Temperature Data Retention test is specifically designed to accelerate charge gain on to or charge loss off of the floating gates in the device's array. Since the charge on these gates determines the actual pattern and function of the device, this test is a measure of the reliability of the device in retaining programmed information. In High Temperature Data Retention, the E^2 cell reliability is determined by monitoring the cell margin after biased static operation at 150°C. All cells in all arrays are life tested in both programmed and erased states.

EE9 Data Retention (HTRX) Conditions:

Stress Duration: 168, 500, 1000, 2000 hours.
Temperature: 150°C
Stress Voltage ispMACH 4000: V_{CC} = 1.95V
Stress Voltage LA-ispMACH 4064V: V_{CC} = 3.6V
Method: Lattice Document # 87-101925 and JESD22-A103C / JESD22-A117A

Table 3.2.1: EE9 High Temperature Data Retention Results

Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
LC4128	Seiko	Lot #1	40	0	0	0	0	80,000
LC4128	Seiko	Lot #2	40	0	0	0	0	80,000
LC4256	Seiko	Lot #1	45	0	0	0	0	90,000
LC4256	Seiko	Lot #3	110	0	0	0	0	220,000
LC4256	Seiko	Lot #4	90	0	0	0	0	180,000
LC4256	Seiko	Lot #5	90	0	0	0	0	180,000
LC4256	UMC	Lot #1	90	0	0			45,000
LC4256	UMC	Lot #2	90	0	0			45,000
LC4256	UMC	Lot #3	90	0	0			45,000
LC4256	UMC	Lot #4	90	0	0			45,000
LC4256	UMC	Lot #5	90	0	0	0		90,000
LC4256	UMC	Lot #6	90	0	0	0		90,000
LC4256	UMC	Lot #1	90	0	0	0		90,000
LA4064V	Seiko	Lot #1	79	0	0	0		79,000
LA4064V	Seiko	Lot #2	79	0	0	0		79,000
LA4064V	Seiko	Lot #3	80	0	0	0		80,000

EE9 Cumulative HTRX Failure Rate = 0 / 1,283
EE9 Cumulative HTRX Device Hours = 1,518,000

EE9 Seiko HTRX Results = 0 / 653
EE9 UMC HTRX Results = 0 / 630

3.3 ispMACH 4000 Product Family Endurance Cycling Data

Endurance testing measures the durability of the device through programming and erase cycles. Endurance testing consists of repeatedly programming and erasing all cells in the array at 25°C to simulate programming cycles the user would perform. This test evaluates the integrity of the thin tunnel oxide through which current passes to program the floating gate in each cell of the array.

EE9 Endurance Cycling Test Conditions:
Stress Duration: 1K, 2K, 3K, 5K, 10K Cycles
Temperature: 25°C
Stress Voltage ispMACH 4000: V_{CC} = 1.8V
Method: Lattice Document # 70-104633 and JESD22-A117A

Table 3.3.1: EE9 Endurance Cycling Results

Product Name	Foundry	Lot #	Qty	1K CYC Result	2K CYC Result	3K CYC Result	5K CYC Result	10K CYC Result	Cumulative Device Cycles
LC4256	Seiko	Lot #3	12	0	0	0	0	0	120,000
LC4256	Seiko	Lot #4	10	0	0	0	0	0	100,000
LC4256	Seiko	Lot #5	10	0	0	0	0	0	100,000
LC4256	UMC	Lot #1	29	0	0	0	0	0	290,000
LC4256	UMC	Lot #2	23	0	0	0	0	0	230,000
LC4256	UMC	Lot #5	10	0	0	0	0	0	100,000
LC4256	UMC	Lot #6	10	0	0	0	0	0	100,000
LC4256	UMC	Lot #1	10	0	0	0	0	0	100,000
LC4256	UMC	Lot #2	10	0	0	0	0	0	100,000

EE9 Cumulative EE Cell Endurance Failure Rate = 0 / 124
EE9 Cumulative EE Cell Endurance Device Cycles = 1,240,000

3.4 ispMACH 4000 Product Family – ESD and Latch UP Data (Commercial/Industrial):

Electrostatic Discharge-Human Body Model (Commercial/Industrial):

ispMACH 4000 product family was tested per the JESD22-A114E Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure and Lattice Procedure # 70-100844.

All units were tested at 25^0C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.1 ispMACH 4000 ESD-HBM Data (Commercial/Industrial):

Device	HBM Passing Voltage	JEDEC HBM Classification
LC4032B-TN44	> 2000 V	Class 2
LC4032V-TN44	> 2000 V	Class 2
LC4032ZC-TN44	> 2000 V	Class 2
LC4032ZE-TN48	> 2000 V	Class 2
LC4032ZE-MN64	> 2000 V	Class 2
LC4064B-TN44	> 2000 V	Class 2
LC4064V-TN44	> 2000 V	Class 2
LC4064ZE-TN48	> 2000 V[A]	Class 2
LC4064ZE- MN64	> 2000 V[A]	Class 2
LC4064B-TN100	> 2000 V	Class 2
LC4064V-TN100	> 2000 V	Class 2
LC4064ZC-TN100	> 2000 V	Class 2
LC4064ZE-TN100[B]	> 2000 V[A]	Class 2
LC4064ZE-TCN100[C]	> 2000 V	Class 2
LC4128ZC-TN100	> 2000 V	Class 2
LC4128ZE-TN100[B]	> 2000 V	Class 2
LC4128ZE-TCN100[C]	> 2000 V	Class 2
LC4128C-TN128	> 2000 V	Class 2
LC4128ZE-TN144[B]	> 2000 V	Class 2
LC4128ZE-TCN144[C]	> 2000 V	Class 2
LC4128ZE-MN144	> 2000 V	Class 2
LC4128ZE-TN144[D]	> 1500 V	Class 1C
LC4128ZE-MN144[D]	> 1600 V	Class 1C
LC4256ZE-TN100	> 1800 V	Class 1C
LC4256ZE-TN100[B]	> 1800 V	Class 1C
LC4256ZE-MN144	> 1900 V	Class 1C
LC4256ZE-TN144[B]	> 1900 V	Class 1C
LC4256ZE-TCN144[C]	> 1900 V	Class 1C
LC4256B-FN256	> 2000 V	Class 2
LC4256V-FN256	> 2000 V	Class 2
LC4384B-FN256	> 2000 V	Class 2
LC4384V-FN256	> 2000 V	Class 2
LC4512B-FN256	> 2000 V	Class 2
LC4512V-FN256	> 2000 V	Class 2
LC4512B-FT256	> 2000 V	Class 2
LC4512V-FT256	> 2000 V	Class 2

HBM classification for Commercial/Industrial products, per JESD22-A114

A: LC4064ZE from UMC >2000V for all pins, all lot #s. LC4064ZE from Seiko with Inspection lot # x122xxxx or later meet >2000V for all pins. LC4064ZE from Seiko with Inspection lot # x121xxxx or earlier pass all HBM test conditions of >2000V except for the following combinations, which pass >700V: Positive Vcc to Vss, negative Vss to Vcc, and negative IOs to Vcc.

B: LC4064ZE- TN100, LC4128ZE-TN100 and LC4128ZE-TN144 and LC4256ZE-TCN144 from Seiko+UTAC: include 0.8mil diameter Au bond wire.

C: LC4064ZE-TCN100, LC4128ZE-TCN100, LC4128ZE-TCN144 and LC4256ZE-TCN144 bill-of-materials include Cu bond wires.

D: LC4128ZE-TN144/MN144, data is on UMC silicon.

Electrostatic Discharge-Charged Device Model (Commercial/Industrial):

ispMACH4000 product family was tested per the JESD22-C101D, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure and Lattice Procedure # 70-100844.

All units were tested at 25°C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.3 ispMACH 4000 ESD-CDM Data (Commercial/Industrial):

Device	CDM Passing Voltage	JEDEC CDM Classification
LC4032B-TN44	> 1000V	Class IV
LC4032V-TN44	> 1000V	Class IV
LC4032ZC-TN44	> 1000V	Class IV
LC4032ZE-TN48	> 1000V	Class IV
LC4032ZE-MN64	> 1000V	Class IV
LC4064B-TN44	> 1000V	Class IV
LC4064V-TN44	> 1000V	Class IV
LC4064ZE-TN48	> 1000V	Class IV
LC4064ZE-MN64	> 1000V	Class IV
LC4064V-TN100	> 1000V	Class IV
LC4064B-TN100	> 1000V	Class IV
LC4064ZC-TN100	> 1000V	Class IV
LC4064ZE-TN100[B]	> 900V	Class III
LC4064ZE-TCN100[C]	> 900V	Class III
LC4128ZC-TN100	> 1000V	Class IV
LC4128ZE-TN100[B]	> 900V	Class III
LC4128ZE-TCN100[C]	> 1000V	Class IV
LC4128C-TN128	> 750V	Class III
LC4128ZE-TN144[B]	> 700V	Class III
LC4128ZE-TN144[D]	> 900V	Class III
LC4128ZE-TCN144[C]	> 800V	Class III
LC4128ZE-MN144	> 1000V	Class IV
LC4256ZE-TN100	> 900V	Class III
LC4256ZE-TN100[B]	> 1000V	Class IV
LC4256ZE-MN144	> 700V	Class III
LC4256ZE-TN144[B]	> 800V	Class III
LC4256ZE-TCN144[C]	> 750V	Class III
LC4256B-FN256	> 750V	Class III
LC4256V-FN256	> 750V	Class III
LC4384B-FN256	> 750V	Class III
LC4384V-FN256	> 600V	Class III
LC4512B-FN256	> 600V	Class III
LC4512V-FN256	> 650V	Class III
LC4512B-FT256	> 650V	Class III

CDM classification for Commercial/Industrial products, per JESD22-C101

B: LC4064ZE- TN100, LC4128ZE-TN100 and LC4128ZE-TN144 and LC4256ZE-TCN144 from Seiko+UTAC: include 0.8mil diameter Au bond wire.

C: LC4064ZE-TCN100, LC4128ZE-TCN100, LC4128ZE-TCN144 and LC4256ZE-TCN144 bill-of-materials include Cu bond wires.

D: LC4128ZE-TN144, data is on UMC silicon.

Latch-Up (Commercial/Industrial):

ispMACH 4000 product family was tested per the JEDEC EIA/JESD78A IC Latch-up Test procedure and Lattice Procedure # 70-101570.

All units were tested at 25°C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Earlier latch-up testing at Lattice was hardware limited to room temperature testing. Additionally, maximum-rated ambient temperature latch-up testing is generally considered to be approximately 2X worse than the trigger values found at room temperature. In order to guard band our room temperature IO latch-up testing the standard was 4X, or +/- 400mA trigger current. Therefore, the previous Lattice I/O LU standard was >400mA at room temperature, while the present standard is >100mA at maximum-rated ambient temperature.

Table 3.4.5 ispMACH4000 I/O Latch Up Data (Commercial/Industrial):

Device	I/O Latch-up Results	Jedec/JESD78 Latch-up Level
LC4032B-TN44	+/- 400mA @ 25°C	Class I, Level B
LC4032V-TN44	+/- 400mA @ 25°C	Class I, Level B
LC4032ZC-TN44	+/- 400mA @ 25°C	Class I, Level B
LC4032ZE-TN48	+/- 100mA @ 125°C	Class II, Level A
LC4064B-TN44	+/- 400mA @ 25°C	Class I, Level B
LC4064V-TN44	+/- 400mA @ 25°C	Class I, Level B
LC4064B-TN100	+/- 100mA @ 105°C	Class II, Level A
LC4064V-TN100	+/- 100mA @ 105°C	Class II, Level A
LC4064ZC-TN100	+/- 400mA @ 25°C	Class I, Level B
LC4064ZE-TN100[B]	+/- 100mA @ 105°C	Class II, Level A
LC4064ZE-TCN100[C]	+/- 100mA @ 105°C	Class II, Level A
LC4128ZE-TN100[B]	+/- 100mA @ 105°C	Class II, Level A
LC4128ZE-TCN100[C]	+/- 100mA @ 105°C	Class II, Level A
LC4128ZC-TN100	+/- 400mA @ 25°C	Class I, Level B
LC4128C-TN128	+/- 400mA @ 25°C	Class I, Level B
LC4128ZE-TN144[B]	+/- 100mA @ 105°C	Class II, Level A
LC4128ZE-TN144[D]	+/- 100mA @ 105°C	Class II, Level A
LC4128ZE-MN144[D]	+/- 100mA @ 105°C	Class II, Level A
LC4128ZE-TCN144[C]	+/- 100mA @ 105°C	Class II, Level A
LC4256ZE-TN100[B]	+/- 100mA @ 105°C	Class II, Level A
LC4256ZE-TN144[B]	+/- 100mA @ 105°C	Class II, Level A
LC4256ZE-TCN144[C]	+/- 100mA @ 105°C	Class II, Level A
LC4256ZE-TN144	+/- 100mA @ 125°C	Class II, Level A
LC4256B-FN256	+/- 400mA @ 25°C	Class I, Level B
LC4256V-FN256	+/- 400mA @ 25°C	Class I, Level B
LC4384B-FN256	+/- 400mA @ 25°C	Class I, Level B
LC4384V-FN256	+/- 400mA @ 25°C	Class I, Level B
LC4512B-FN256	+/- 100mA @ 125°C	Class II, Level A
LC4512V-FN256	+/- 100mA @ 125°C	Class II, Level A
LC4512B-FT256	+/- 100mA @ 105°C	Class II, Level A
LC4512V-FT256	+/- 100mA @ 105°C	Class II, Level A

Latch up classification for Commercial/Industrial products, per JESD78

B: LC4064ZE- TN100, LC4128ZE-TN100 and LC4128ZE-TN144 and LC4256ZE-TCN144 from Seiko+UTAC: include 0.8mil diameter Au bond wire.

C: LC4064ZE-TCN100, LC4128ZE-TCN100, LC4128ZE-TCN144 and LC4256ZE-TCN144 bill-of-materials include Cu bond wires.

D: LC4128ZE-TN144/MN144, data is on UMC silicon.

Table 3.4.6 ispMACH4000 V-Supply (Over Voltage) Latch Up Data (Commercial/Industrial):

Device	V-supply Over-Voltage LU	Jedec/JESD78 Latch-up Level
LC4032ZE-TN48	> 1.5X V-supply @ 125°C	Class II
LC4064V-TN100	> 1.5X V-supply @ 105°C	Class II
LC4064B-TN100	> 1.5X V-supply @ 105°C	Class II
LC4064ZE-TN100[B]	> 1.5X V-supply @ 105°C	Class II
LC4064ZE-TCN100[C]	> 1.5X V-supply @ 105°C	Class II
LC4128ZE-TN100[B]	> 1.5X V-supply @ 105°C	Class II
LC4128ZE-TCN100[C]	> 1.5X V-supply @ 105°C	Class II
LC4128ZE-TN144[B]	> 1.5X V-supply @ 105°C	Class II
LC4128ZE-TN144[D]	> 1.5X V-supply @ 105°C	Class II
LC4128ZE-MN144[D]	> 1.5X V-supply @ 105°C	Class II
LC4128ZE-TCN144[C]	> 1.5X V-supply @ 105°C	Class II
LC4256ZE-TN100[B]	> 1.5X V-supply @ 105°C	Class II
LC4256ZE-TN144[B]	> 1.5X V-supply @ 105°C	Class II
LC4256ZE-TCN144[C]	> 1.5X V-supply @ 105°C	Class II
LC4256B-FN256	> 1.5X V-supply @ 125°C	Class II
LC4256V-FN256	> 1.5X V-supply @ 125°C	Class II
LC4384B-FN256	> 1.5X V-supply @ 125°C	Class II
LC4384V-FN256	> 1.5X V-supply @ 125°C	Class II
LC4512B-FN256	> 1.5X V-supply @ 125°C	Class II
LC4512V-FN256	> 1.5X V-supply @ 125°C	Class II
LC4512B-FT256	> 1.5X V-supply @ 105°C	Class II
LC4512V-FT256	> 1.5X V-supply @ 105°C	Class II

Latch up classification for Commercial/Industrial products, per JESD78

B: LC4064ZE- TN100, LC4128ZE-TN100 and LC4128ZE-TN144 and LC4256ZE-TCN144 from Seiko+UTAC: include 0.8mil diameter Au bond wire.

C: LC4064ZE-TCN100, LC4128ZE-TCN100, LC4128ZE-TCN144 and LC4256ZE-TCN144 bill-of-materials include Cu bond wires.

D: LC4128ZE-TN144/MN144, data is on UMC silicon.

3.5 LA-ispMACH 4000V/Z Product Family – ESD and Latch UP Data (Automotive):

LA-ispMACH4000V Automotive Grade product family was tested and classified per the AEC-Q100-002-Rev-D Human Body Model (HBM) Electrostatic Discharge (ESD) Test criteria and the JESD22-A114C.01 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure.

All units were tested at 25°C and +125°C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.2 LA-ispMACH 4000 ESD-HBM Data (Automotive):

Device	HBM Passing Voltage	AEC-Q100-002 HBM Classification
LA4032V-TN44	> 2000 V	H2
LA4032ZC-TN48	> 2000 V	H2
LA4064V-TN100	> 2000 V	H2
LA4064ZC-TN100	> 2000 V	H2
LA4128V-TN100	> 2000 V	H2
LA4128ZC-TN100	> 2000 V	H2
LA4128V-TN144	> 2000 V	H2

HBM classification for Automotive products, per AEC-Q100-002-Rev-D

LA-ispMACH4000 Automotive Grade product family was tested and Classified per the AEC-Q100-011-Rev-B, Charge Device Model (CDM) Electrostatic Discharge Test criteria and the JESD22-C101C, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure.

All units were tested at 25°C and +125°C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.4 LA-ispMACH 4000 ESD-CDM Data (Automotive):

Device	CDM Passing Voltage	AEC-Q100-011 Classification
LA4032V-TN44	> 1000V	C5
LA4032ZC-TN48	> 1000V	C5
LA4064V-TN100	> 1000V	C5
LA4064ZC-TN100	> 1000V	C5
LA4128V-TN100	> 750V	C4
LA4128ZC-TN100	> 750V	C4
LA4128V-TN144	> 750V	C4

CDM classification for Commercial/Industrial products, per AEC-Q100-011

LA-ispMACH4000V/ZC Automotive Grade product family was tested per the AEC-Q100-004-Rev-C, IC Latch-up Test criteria and JEDEC EIA/JESD78 IC Latch-up Test procedure.

All units were tested at 25°C and +125°C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.7 LA-ispMACH4000 I/O Latch Up Data (Automotive):

Device	I/O Latch-up Results	Jedec/JESD78 Latch-up Level
LA4032V-TN44	+/- 100mA @ 125°C	Class II, Level A
LA4032ZC-TN48	+/- 100mA @ 125°C	Class II, Level A
LA4064V-TN100	+/- 100mA @ 125°C	Class II, Level A
LA4064ZC-TN100	+/- 100mA @ 125°C	Class II, Level A
LA4128V-TN100	+/- 100mA @ 125°C	Class II, Level A
LA4128ZC-TN100	+/- 100mA @ 125°C	Class II, Level A
LA4128V-TN144	+/- 100mA @ 125°C	Class II, Level A

4.0 PACKAGE QUALIFICATION DATA FOR ispMACH 4000 FAMILIES

The ispMACH 4000 product family is offered in ftBGA, csBGA, and TQFP packages. To cover the range of die in the largest package types for this product family, different package and die combinations were chosen as the generic qualification vehicles for all the package qualification tests including, Temperature Cycling (T/C), Un-biased HAST (UHAST)and Biased HAST (BHAST). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual inspection.

The generation and use of generic data is applied across a family of products or packages emanating from one base wafer foundry or assembly process is a Family Qualification, or Qualification By Extension. For the package stresses BHAST and UHAST, these are considered generic for a given Package Technology. T/C is considered generic up to an evaluated die size + package size + 10%, for a given Package Technology. Surface Mount Pre-Conditioning (SMPC) is considered generic up to an evaluated Peak Reflow temperature, for a given Package Technology. The following tables demonstrate the package qualification matrix.

Table 4.1 ispMACH 4000 Product-Package Qualification-By-Extension Matrix

Product	Stress Test	ASEM / ATK / UNISEM /UTAC Au-Wire Leaded Packages						ASEM	ASEM / ATP / UNISEM / UTAC		ASEM / UTAC	ASEM / ATP
		44-TQFP	48-TQFP	100-TQFP	128-TQFP	144-TQFP	176-TQFP	64-ucBGA	56-csBGA	132-csBGA	256-ftBGA	** 256-fpBGA
LC4512-V/B/C	SMPC	Package not offered	Package not offered	Package not offered	Package not offered	Package not offered	**MSL3**	Package not offered	Package not offered	Package not offered	**MSL3**	**MSL3**
	T/C						**1k cyc**				**1k cyc**	**1k cyc**
	BHAST						By Ext				**96 hrs**	By Ext
	UHAST						By Ext				**96 hrs**	By Ext
	* HTSL						By Ext				By Ext	By Ext
LC4384-V/B/C	SMPC	Package not offered	Package not offered	Package not offered	Package not offered	Package not offered	**MSL3**	Package not offered	Package not offered	Package not offered	By Ext	By Ext
	T/C						**1k cyc**				By Ext	By Ext
	BHAST						By Ext				By Ext	By Ext
	UHAST						By Ext				By Ext	By Ext
	* HTSL						By Ext				By Ext	By Ext
LC4256-V/B/C/ ZC/ZE	SMPC	Package not offered	Package not offered	By Ext	Package not offered	**MSL3**	**MSL3**	Package not offered	Package not offered	**MSL3**	By Ext	By Ext
	T/C			By Ext		**1k cyc**	**1k cyc**			**1k cyc**	By Ext	By Ext
	BHAST			By Ext		**96 hrs**	**96 hrs**			**96 hrs**	By Ext	By Ext
	UHAST			By Ext		**96 hrs**	**96 hrs**			**96 hrs**	By Ext	By Ext
	* HTSL			By Ext		**1k hrs**	**1k hrs**			By Ext	By Ext	**1k hrs**
LC4128-V/B/C/ ZC/ZE	SMPC	Package not offered	Package not offered	By Ext	**MSL3**	**MSL3**	Package not offered	Package not offered	Package not offered	By Ext	Package not offered	Package not offered
	T/C			By Ext	**1k cyc**	**1k cyc**				By Ext		
	BHAST			By Ext	By Ext	**96 hrs**				By Ext		
	UHAST			By Ext	By Ext	**96 hrs**				By Ext		
	* HTSL			By Ext	By Ext	**1k hrs**				By Ext		
LC4064-V/B/C/ ZC/ZE	SMPC	**MSL3**	By Ext	**MSL3**	Package not offered	Package not offered	Package not offered	**MSL3**	By Ext	By Ext	Package not offered	Package not offered
	T/C	**1k cyc**	By Ext	**1k cyc**				**1k cyc**	By Ext	By Ext		
	BHAST	**96 hrs**	By Ext	By Ext				By Ext	By Ext	By Ext		
	UHAST	**96 hrs**	By Ext	By Ext				**96 hrs**	By Ext	By Ext		
	* HTSL	By Ext	By Ext	By Ext				By Ext	By Ext	By Ext		
LC4032-V/B/C/ ZC/ZE	SMPC	By Ext	**MSL3**	Package not offered	Package not offered	Package not offered	Package not offered	By Ext	By Ext	Package not offered	Package not offered	Package not offered
	T/C	By Ext	**1k cyc**					By Ext	By Ext			
	BHAST	By Ext	By Ext					By Ext	By Ext			
	UHAST	By Ext	By Ext					By Ext	By Ext			
	* HTSL	By Ext	By Ext					By Ext	By Ext			

* Package HTSL stress run as HTRX (data retention). Both stresses are 1000 hour 150°C bakes.
** Package no longer offered. Use 256 ftBGA for all new designs. Refer to PCN#14A-07 for 256 fpBGA package discontinuance.
Note: All packages are qualified by an extension from the largest package and largest die in that package technology.

Table 4.2 LA-ispMACH 4000 (Automotive) Product-Package Qualification-By-Extension Matrix

Product	Stress Test	ASEM / ATK Au-Wire Wire Leaded Packages				
		44-TQFP TN44	48-TQFP TN48	100-TQFP TN100	128-TQFP TN128	144-TQFP TN144
LA4128V/ZC	SMPC	Package not offered	Package not offered	"V/ZC" Qualified by extension	"V" Qualified by extension	MSL3/260C
	T/C					1k cycles
	BHAST					96 hours
	UHAST					96 hours
	HTSL					By extension
LA4064V/ZC	SMPC	"V" Qualified by extension	"V/ZC" Qualified by extension	"V/ZC" Qualified by extension	Package not offered	Package not offered
	T/C					
	BHAST					
	UHAST					
	HTSL			1k hours		
LA4032V/ZC	SMPC	"V" Qualified by extension	"V/ZC" Qualified by extension	Package not offered	Package not offered	Package not offered
	T/C					
	BHAST					
	UHAST					
	HTSL					

Note: All packages are qualified by an extension from the largest package and largest die in that package technology.

Table 4.3 ispMACH 4000ZE Copper (Cu) Bond Wire Product-Package Qualification-By-Extension Matrix

Product	Stress Test	ASEM / UTAC Cu-Wire Leaded Packages			
		44-TQFP TCN44	48-TQFP TCN48	100-TQFP TCN100	144-TQFP TCN144
LC4256ZE	SMPC	Package not offered	Package not offered	Qualified by extension	MSL3/260C
	T/C				1k cycles
	BHAST				96 hours
	UHAST				96 hours
	HTSL				1k hours
LC4128ZE	SMPC	Package not offered	Package not offered	Qualified by extension	Qualified by extension
	T/C				
	BHAST				
	UHAST				
	HTSL				
LC4064ZE	SMPC	Qualified by extension	Qualified by extension	Package not offered	Package not offered
	T/C				
	BHAST				
	UHAST				
	HTSL				

4.1 ispMACH 4000 Product Family Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JEDEC JESD22-A113 "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3(MSL3) package moisture sensitivity and dry-pack storage requirements.

Surface Mount Preconditioning (MSL3)
(10 Temperature Cycles between -55°C and 125°C, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, 225/245/250/260 °C Reflow Simulation, 3 passes) performed before all EE9 package tests.
MSL3 Packages: TQFP, fpBGA, ftBGA, csBGA, ucBGA

Surface Mount Preconditioning (MSL2)
(10 Temperature Cycles between -55°C and 125°C, 24 hours bake @ 125°C, 85°C/60% RH, soak 168 hours, 260°C Reflow Simulation, 3 passes) performed before all EE9 package tests.
MSL2 Packages: csBGA

Method: Lattice Procedure # 70-103467, J-STD-020 and JESD22-A113

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LC4032ZC	48 TQFP	Amkor	Lot #1	47	0	260°C
LC4032ZC	48 TQFP	Amkor	Lot #2	47	0	260°C
LC4032ZE	48 TQFP	Amkor	Lot #1	45	0	260°C
LC4032ZE	48 TQFP	Amkor	Lot #2	45	0	260°C
LC4064ZC	100 TQFP	Amkor	Lot #1	45	0	260°C
LC4064ZC	100 TQFP	Amkor	Lot #2	45	0	260°C
LC4064ZE	64 ucBGA	ASEM	Lot #1	154	0	260°C
LC4064ZE	64 ucBGA	ASEM	Lot #2	154	0	260°C
LC4128	128 TQFP	Amkor	Lot #1	45	0	260°C
LC4128	128 TQFP	Amkor	Lot #2	45	0	260°C
LC4256	176 TQFP	Amkor	Lot #1	135	0	260°C
LC4256	176 TQFP	Amkor	Lot #2	135	0	260°C
LC4256	176 TQFP	Amkor	Lot #3	135	0	260°C
LC4032	44 TQFP	ASEM	Lot #1	45	0	260°C
LC4064	44 TQFP	Amkor	Lot #1	45	0	260°C
LC4064	100 TQFP	Amkor	Lot #2	45	0	260°C
LC4128	128 TQFP	Amkor	Lot #1	45	0	260°C
LC4256	176 TQFP	Amkor	Lot #1	141	0	260°C
LC4256	176 TQFP	Amkor	Lot #2	141	0	260°C
LC4256	176 TQFP	Amkor	Lot #3	141	0	260°C
LC4256	256 fpBGA	Amkor	Lot #1	45	0	260°C
LC4384	176 TQFP	Amkor	Lot #1	45	0	260°C

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LC4512	176 TQFP	Amkor	Lot #1	45	0	260°C
LC4512	176 TQFP	Amkor	Lot #2	45	0	260°C
LC4256	132 csBGA	ASEM	Lot #1	100	0	240°C
LC4256	132 csBGA	ASEM	Lot #2	100	0	240°C
LC4256	132 csBGA	ASEM	Lot #3	100	0	240°C
LC4256	132 csBGA	ASEM	Lot #1	50	0	260°C
LC4256	132 csBGA	ASEM	Lot #2	50	0	260°C
LC4256	132 csBGA	ASEM	Lot #3	50	0	260°C
LC4256	132 csBGA[A]	ASEM	Lot #1	50	0	260°C
LC4256	132 csBGA[A]	ASEM	Lot #2	50	0	260°C
LC4512	176 TQFP	ASEM	Lot #1	150	0	260°C
LC4512	176 TQFP	ASEM	Lot #2	150	0	260°C
LC4512	176 TQFP	ASEM	Lot #3	150	0	260°C
LC4512	176 TQFP	Amkor	Lot #1	150	0	260°C
LC4512	176 TQFP	Amkor	Lot #2	150	0	260°C
LC4512	176 TQFP	Amkor	Lot #3	150	0	260°C
LC45256ZC	132 csBGA	UNISEM	Lot #1	120	0	260°C
LC45256ZC	132 csBGA	UNISEM	Lot #2	120	0	260°C
LC45256ZC	132 csBGA	UNISEM	Lot #3	120	0	260°C
LC45256ZC	132 csBGA	UNISEM	Lot #4	167	0	260°C
LC45256ZC	132 csBGA	UNISEM	Lot #5	167	0	260°C
LC45256ZC	132 csBGA	UNISEM	Lot #6	167	0	260°C
LC4064	44 TQFP	UNISEM	Lot #1	145	0	260°C
LC4064	44 TQFP	UNISEM	Lot #2	145	0	260°C
LC4064	44 TQFP	UNISEM	Lot #3	145	0	260°C
LC4512	176 TQFP	UNISEM	Lot #1	99	0	260°C
LC4512	176 TQFP	UNISEM	Lot #2	98	0	260°C
LC4512	176 TQFP	UNISEM	Lot #3	75	0	260°C
LCMXO2280	256 ftBGA[C]	ASEM	Lot #1	45	0	260°C
LCMXO2280	256 ftBGA[C]	ASEM	Lot #2	45	0	260°C
ispLSI 5384VE	256 ftBGA[C]	ASEM	Lot #1	77	1[B]	260°C
isplSI 5384VE	256 ftBGA[C]	ASEM	Lot #2	77	0	260°C
isplSI 5384VE	256 ftBGA[C]	UTAC	Lot #1	199	0	260°C
isplSI 5384VE	256 ftBGA[C]	UTAC	Lot #2	199	0	260°C
isplSI 5384VE	256 ftBGA[C]	UTAC	Lot #3	231	0	260°C
LA4128V	144 TQFP	ASEM	Lot #1	234	0	260°C
LA4128V	144 TQFP	ASEM	Lot #2	231	0	260°C
LA4128V	144 TQFP	ASEM	Lot #3	234	0	260°C
LA4128V	144 TQFP	Amkor	Lot #1	81	0	260°C
LA4128V	144 TQFP	Amkor	Lot #2	82	0	260°C

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LA4128V	144 TQFP	Amkor	Lot #3	78	0	260°C
LA4128V	144 TQFP	Amkor	Lot #4	162	0	260°C
LA4128V	144 TQFP	Amkor	Lot #5	200	0	260°C
LA4128V	144 TQFP	Amkor	Lot #6	200	0	260°C
LC4256ZE	TN 144[D]	UTAC	Lot #1	319	0	260°C
LC4256ZE	TN 144[D]	UTAC	Lot #2	319	0	260°C
LC4256ZE	TN 144[D]	UTAC	Lot #3	319	0	260°C
LC4256ZE	TCN 144[E]	UTAC	Lot #1	319	0	260°C
LC4256ZE	TCN 144[E]	UTAC	Lot #2	319	0	260°C
LC4256ZE	TCN 144[E]	UTAC	Lot #3	319	0	260°C

Cumulative SMPC Failure Rate = 1 / 9,167

A: MSL-2 packages

B: Functional failure after SMPC CAR# 2700

C: The LCMXO2280 and ispLSI 5384VE were the qualification vehicles for ASEM & UTAC 256 ftBGA packages. The other ASEM & UTAC Mach4K 256 ftBGA packages are qualified by extension.

D: The LC4256ZE, TN144 bill-of-materials includes 0.8mil Gold (Au) bond wires.

E: The LC4256ZE, TCN144 bill-of-materials includes 0.8mil Copper (Cu) bond wires.

4.2 ispMACH 4000 Product Family Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104 "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, fpBGA, ftBGA, csBGA, ucBGA
Stress Duration: 1000 cycles
Stress Conditions: Temperature cycling between -55°C to 125°C
Method: Lattice Procedure # 70-101568 and JESD22-A104C

Table 4.2.1: Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Quantity	250 Cycles	500 Cycles	1000 Cycles
LC4032ZC	48 TQFP	Amkor	Lot #1	47	0	0	0
LC4032ZC	48 TQFP	Amkor	Lot #2	47	0	0	0
LC4032ZE	48 TQFP	Amkor	Lot #1	45	0	0	0
LC4032ZE	48 TQFP	Amkor	Lot #2	45	0	0	0
LC4064ZC	10 TQFP	Amkor	Lot #1	45	0	0	0
LC4064ZC	100 TQFP	Amkor	Lot #2	45	0	0	0
LC4064ZE	64 ucBGA	ASEM	Lot #1	77	0	0	0
LC4064ZE	64 ucBGA	ASEM	Lot #2	77	0	0	0
LC4128	128 TQFP	Amkor	Lot #1	45	0	0	0
LC4128	128 TQFP	Amkor	Lot #2	45	0	0	0
LC4256	176 TQFP	Amkor	Lot #1	45	0	0	0
LC4256	176 TQFP	Amkor	Lot #2	45	0	0	0
LC4256	176 TQFP	Amkor	Lot #3	45	0	0	0
LC4032	44 TQFP	Amkor	Lot #1	45	0	0	0
LC4064	100 TQFP	Amkor	Lot #2	45	0	0	0
LC4128	128 TQFP	Amkor	Lot #1	45	0	0	0
LC4256	176 TQFP	Amkor	Lot #1	45	0	0	0
LC4256	176 TQFP	Amkor	Lot #2	45	0	0	0
LC4256	176 TQFP	Amkor	Lot #3	45	0	0	0
LC4256	256 fpBGA	Amkor	Lot #1	45	0	0	0
LC4384	176 TQFP	Amkor	Lot #1	45	0	0	0
LC4512	176 TQFP	Amkor	Lot #1	45	0	0	0
LC4512	176 TQFP	Amkor	Lot #2	45	0	0	0
LC4256	132 csBGA	ASEM	Lot #1	50	0	0	0
LC4256	132 csBGA	ASEM	Lot #2	50	0	0	0
LC4256	132 csBGA	ASEM	Lot #3	48	0	0	0
LC4256	132 csBGA	ASEM	Lot #1	48	0	0	0
LC4256	132 csBGA	ASEM	Lot #2	50	0	0	0
LC4256	132 csBGA	ASEM	Lot #3	50	0	0	0
LC4256	132 csBGA[A]	ASEM	Lot #1	50	0	0	0
LC4256	132 csBGA[A]	ASEM	Lot #2	50	0	0	0

Product Name	Package	Assembly Site	Lot Number	Quantity	250 Cycles	500 Cycles	1000 Cycles
LC4512	176 TQFP	ASEM	Lot #1	50	0	0	0
LC4512	176 TQFP	ASEM	Lot #2	50	0	0	0
LC4512	176 TQFP	ASEM	Lot #3	50	0	0	0
LC4512	176 TQFP	Amkor	Lot #1	45	0	0	0
LC4512	176 TQFP	Amkor	Lot #2	45	0	0	0
LC4512	176 TQFP	Amkor	Lot #3	45	0	0	0
LC45256ZC	132 csBGA	UNISEM	Lot #1	120	0	0	0
LC45256ZC	132 csBGA	UNISEM	Lot #2	120	0	0	0
LC45256ZC	132 csBGA	UNISEM	Lot #3	120	0	0	0
LC4064	44 TQFP	UNISEM	Lot #1	45	0	0	0
LC4064	44 TQFP	UNISEM	Lot #2	45	0	0	0
LC4064	44 TQFP	UNISEM	Lot #3	45	0	0	0
LC4512	176 TQFP	UNISEM	Lot #1	50	0	0	0
LC4512	176 TQFP	UNISEM	Lot #2	49	0	0	0
LC4512	176 TQFP	UNISEM	Lot #3	45	0	0	0
LCMXO2280	256 ftBGA[B]	ASEM	Lot #1	45	0	0	0
LCMXO2280	256 ftBGA[B]	ASEM	Lot #2	45	0	0	0
ispLSI 5384VE	256 ftBGA[B]	ASEM	Lot #1	76	0	0	0
isplSI 5384VE	256 ftBGA[B]	ASEM	Lot #2	77	0	0	0
isplSI 5384VE	256 ftBGA[B]	UTAC	Lot #1	77	0	0	0
isplSI 5384VE	256 ftBGA[B]	UTAC	Lot #2	77	0	0	0
isplSI 5384VE	256 ftBGA[B]	UTAC	Lot #3	77	0	0	0
LA4128V	144 TQFP	ASEM	Lot #1	77	0	0	0
LA4128V	144 TQFP	ASEM	Lot #2	77	0	0	0
LA4128V	144 TQFP	ASEM	Lot #3	77	0	0	0
LA4128V	144 TQFP	Amkor	Lot #1	81	0	0	0
LA4128V	144 TQFP	Amkor	Lot #2	82	0	0	0
LA4128V	144 TQFP	Amkor	Lot #3	78	0	0	0
LC4256ZE	TN 144[C]	UTAC	Lot #1	83	0	0	0
LC4256ZE	TN 144[C]	UTAC	Lot #2	83	0	0	0
LC4256ZE	TN 144[C]	UTAC	Lot #3	83	0	0	0
LC4256ZE	TCN 144[D]	UTAC	Lot #1	83	0	0	0
LC4256ZE	TCN 144[D]	UTAC	Lot #2	83	0	0	0
LC4256ZE	TCN 144[D]	UTAC	Lot #3	83	0	0	0

Cumulative Temp Cycle Failure Rate = 0 / 3,867

A: MSL-2 packages

B: The LCMXO2280 and ispLSI 5384VE were the qualification vehicles for ASEM & UTAC 256 ftBGA packages. The other ASEM & UTAC Mach4K 256 ftBGA packages are qualified by extension.

C: The LC4256ZE, TN144 bill-of-materials includes 0.8mil Gold (Au) bond wires.

D: The LC4256ZE, TCN144 bill-of-materials includes 0.8mil Copper (Cu) bond wires.

4.3 ispMACH 4000 Product Family Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent JEDEC JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," for which the conditions are 96 hour exposure at 130°C and 85% relative humidity. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, fpBGA, ftBGA, csBGA, ucBGA
Stress Duration: 96 Hrs
Stress Conditions: 130°C, 15psig, 85% RH
Method: Lattice Procedure # 70-104285 and JESD22-A118

Table 4.3.1: Unbiased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LC4064ZE	64 ucBGA	ASEM	Lot #1	77	0	96 Hrs
LC4064ZE	64 ucBGA	ASEM	Lot #2	77	0	96 Hrs
LC4256	176 TQFP	ASEM	Lot #1	45	0	96 Hrs
LC4256	176 TQFP	ASEM	Lot #2	45	0	96 Hrs
LC4256	176 TQFP	ASEM	Lot #3	45	0	96 Hrs
LC4256	176 TQFP	Amkor	Lot #1	45	0	96 Hrs
LC4256	176 TQFP	Amkor	Lot #2	45	0	96 Hrs
LC4256	176 TQFP	Amkor	Lot #3	45	0	96 Hrs
LC45256ZC	132 csBGA	UNISEM	Lot #4	45	0	96 Hrs
LC45256ZC	132 csBGA	UNISEM	Lot #5	45	0	96 Hrs
LC45256ZC	132 csBGA	UNISEM	Lot #6	45	0	96 Hrs
LC4512	176 TQFP	Amkor	Lot #1	45	0	96 Hrs
LC4512	176 TQFP	Amkor	Lot #2	45	0	96 Hrs
LC4512	176 TQFP	Amkor	Lot #3	45	0	96 Hrs
LC4064	44 TQFP	UNISEM	Lot #1	50	0	96 Hrs
LC4064	44 TQFP	UNISEM	Lot #2	50	0	96 Hrs
LC4064	44 TQFP	UNISEM	Lot #3	50	0	96 Hrs
LC4512	176 TQFP	UNISEM	Lot #1	49	0	96 Hrs
LC4512	176 TQFP	UNISEM	Lot #2	49	0	96 Hrs
LC4512	176 TQFP	UNISEM	Lot #3	30	0	96 Hrs
isplSI 5384VE	256 ftBGA[A]	UTAC	Lot #1	77	0	96 Hrs
isplSI 5384VE	256 ftBGA[A]	UTAC	Lot #2	77	0	96 Hrs
isplSI 5384VE	256 ftBGA[A]	UTAC	Lot #3	77	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #1	77	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #2	75	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #3	77	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #4	81	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #5	100	0	96 Hrs

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LA4128V	144 TQFP	Amkor	Lot #6	100	0	96 Hrs
LC4256ZE	TN 144[B]	UTAC	Lot #1	77	0	96 Hrs
LC4256ZE	TN 144[B]	UTAC	Lot #2	77	0	96 Hrs
LC4256ZE	TN 144[B]	UTAC	Lot #3	77	0	96 Hrs
LC4256ZE	TCN 144[C]	UTAC	Lot #1	77	0	96 Hrs
LC4256ZE	TCN 144[C]	UTAC	Lot #2	77	0	96 Hrs
LC4256ZE	TCN 144[C]	UTAC	Lot #3	77	0	96 Hrs

Cumulative Unbiased HAST failure Rate = 0 / 2,175

A: The LCMXO2280 and ispLSI 5384VE were the qualification vehicles for ASEM & UTAC 256 ftBGA packages. The other ASEM & UTAC Mach4K 256 ftBGA packages are qualified by extension.

B: The LC4256ZE, TN144 bill-of-materials includes 0.8mil Gold (Au) bond wires.

C: The LC4256ZE, TCN144 bill-of-materials includes 0.8mil Copper (Cu) bond wires.

4.4 ispMACH 4000 Product Family THB: Biased HAST Data

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD A110-B "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are with Vcc bias and alternate pin biasing in an ambient of 130°C and 85% relative humidity. Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, fpBGA, ftBGA, csBGA, ucBGA
Stress Conditions: Vcc= 1.95V/ 3.6V, 130°C / 85% RH, 15 psig
Stress Duration: 96 hours
Method: Lattice Procedure # 70-101571 and JESD22-A101B

Table 4.4.1: Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LC4256	176 TQFP	Amkor	Lot #1	45	0	96 Hrs
LC4256	176 TQFP	Amkor	Lot #2	45	0	96 Hrs
LC4256	176 TQFP	Amkor	Lot #3	45	0	96 Hrs
LC4256	176 TQFP	Amkor	Lot #1	45	0	96 Hrs
LC4256	176 TQFP	Amkor	Lot #2	45	0	96 Hrs
LC4256	176 TQFP	Amkor	Lot #3	45	0	96 Hrs
LC4256	132 csBGA	ASEM	Lot #1	45	0	96 Hrs
LC4256	132 csBGA	ASEM	Lot #2	45	0	96 Hrs
LC4256	132 csBGA	ASEM	Lot #3	45	0	96 Hrs
LC4256	176 TQFP	Amkor	Lot #1	45	0	96 Hrs
LC4256	176 TQFP	Amkor	Lot #2	45	0	96 Hrs
LC4256	176 TQFP	Amkor	Lot #3	45	0	96 Hrs
LC45256ZC	132 csBGA	UNISEM	Lot #4	45	0	96 Hrs
LC45256ZC	132 csBGA	UNISEM	Lot #5	45	0	96 Hrs
LC45256ZC	132 csBGA	UNISEM	Lot #6	45	0	96 Hrs
LC4064	44 TQFP	UNISEM	Lot #1	50	0	96 Hrs
LC4064	44 TQFP	UNISEM	Lot #2	50	0	96 Hrs
LC4064	44 TQFP	UNISEM	Lot #3	50	0	96 Hrs
isplSI 5384VE	256 ftBGA[B]	UTAC	Lot #1	45	0	96 Hrs
isplSI 5384VE	256 ftBGA[B]	UTAC	Lot #2	45	0	96 Hrs
isplSI 5384VE	256 ftBGA[B]	UTAC	Lot #3	77	1[A]	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #1	80	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #2	77	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #3	80	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #4	81	0	96 Hrs

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LA4128V	144 TQFP	Amkor	Lot #5	100	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #6	100	0	96 Hrs
LC4256ZE	TN 144[C]	UTAC	Lot #1	77	0	96 Hrs
LC4256ZE	TN 144[C]	UTAC	Lot #2	77	0	96 Hrs
LC4256ZE	TN 144[C]	UTAC	Lot #3	77	0	96 Hrs
LC4256ZE	TCN 144[D]	UTAC	Lot #1	77	0	96 Hrs
LC4256ZE	TCN 144[D]	UTAC	Lot #2	77	0	96 Hrs
LC4256ZE	TCN 144[D]	UTAC	Lot #3	77	0	96 Hrs

Cumulative BHAST failure Rate EE9 = 1 / 1,972

A: Failed for open. CAR # 2699

B: The LCMXO2280 and ispLSI 5384VE were the qualification vehicles for ASEM & UTAC 256 ftBGA packages. The other ASEM & UTAC Mach4K 256 ftBGA packages are qualified by extension.

C: The LC4256ZE, TN144 bill-of-materials includes 0.8mil Gold (Au) bond wires.

D: The LC4256ZE, TCN144 bill-of-materials includes 0.8mil Copper (Cu) bond wires.

4.5 ispMACH 4000 Product Family High Temperature Storage Life (HTSL)

High Temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices. Units were stressed per JESD22-A103C, High Temperature Storage Life. For the original ispMACH 4000 non-volatile based products, the HTRX and HTSL stress and test conditions condition were the same. Therefore in many cases the HTSL test was covered by HTRX. Prior to HTSL testing, all devices are subjected to Surface Mount Preconditioning.

The High Temperature Storage Life units were stressed at 150°C.

High Temperature Storage Life (HTSL) Conditions:
Stress Duration: 168, 500, 1000, 1500 hours.
Temperature: 150°C
Method: Lattice Document # 87-101925 and JESD22-A103C / JESD22-A117A

Table 3.2.2: High Temperature Storage Life Results

Product Name	Package	Assembler	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	1500 Hrs Result	Cumulative Hours
LA4064V	100 TQFP	ASEM	Lot #1	78	0	0	0		78,000
LA4064V	100 TQFP	ASEM	Lot #2	77	0	0	0		77,000
LA4064V	100 TQFP	ASEM	Lot #3	78	0	0	0		78,000
LA4064V	100 TQFP	Amkor	Lot #2	79	0	0	0	0	118,500
LC4256ZE	TN 144[A]	UTAC	Lot #1	83	0	0	0		83,000
LC4256ZE	TN 144[A]	UTAC	Lot #2	83	0	0	0		83,000
LC4256ZE	TN 144[A]	UTAC	Lot #3	83	0	0	0		83,000
LC4256ZE	TCN 144[B]	UTAC	Lot #1	77	0	0	0		77,000
LC4256ZE	TCN 144[B]	UTAC	Lot #2	77	0	0	0		77,000
LC4256ZE	TCN 144[B]	UTAC	Lot #3	77	0	0	0		77,000

EE9 Cumulative HTSL Failure Rate = 0 / 792
EE9 Cumulative HTSL Device Hours = 831,500

A: The LC4256ZE, TN144 bill-of-materials includes 0.8mil Gold (Au) bond wires.

B: The LC4256ZE, TCN144 bill-of-materials includes 0.8mil Copper (Cu) bond wires.

5.0 ispMACH 4000 Process Reliability Wafer Level Review

Several key fabrication process related parameters have been identified by the foundry that would affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. Normal operating conditions are defined in the Electrical Design Rules (EDR). These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence. SM is not an issue for the EE9 BEOL (etched Al lines, W plug Vias, SiO IMD).

Table 5.1 – Wafer Level Reliability Results for Seiko EE9 (180nm) Process Technology

HCI

Device	LVN
delta Ids	-10%
Celsius	25
Vgstress	Vd/2
Vds	2
TTF	5 lots>23yr

TDDB

Device	LVPwell
Celsius	130
Vg	2
Area	8000um²
0.1% TTF	5 lots>133yr

EML

Layer	M1	M2	M3	M4	M5
Celsius	130	130	130	130	130
delta R	20%	20%	20%	20%	20%
Jmax	.573mA/um²	.705mA/um²	.705mA/um²	.705mA/um²	1.233mA/um²
0.1%TTF	4 lots>41yr	4 lots>32yr	4 lots>33yr	4 lots>16yr	5 lots>15yr

Note: Reliability life times are based on listed temperature and used conditions. Detailed WLR test conditions are available upon request.

Table 5.2 – Wafer Level Reliability Results for UMC EE9 (180nm) Process Technology

HCI

Device	LVN	LVP	HVN
delta Ids	-10%	-10%	-10%
Celsius	25	25	25
Vgstress	Vd/2	0	Vd/2
Vds	2	-2	3.6
TTF	12 lots>15yr	6 lots>1200yr	6 lots>28yr

TDDB

Device	LVPwell	LVNwell	HVPwell	HVNwell
Celsius	130	130	130	130
Vg	2	-2	3.6	-3.6
Area	8000um²	8000um²	8000um²	8000um²
0.1% TTF	6 lots>110000yr	6 lots>2300yr	6 lots>76yr	6 lots>70yr

EML

Layer	M1	M2	M3	M4	M5
Celsius	130	130	130	130	130
delta R	+20%	+20%	+20%	+20%	+20%
Jmax	.573mA/um²	.705mA/um²	.705mA/um²	.705mA/um²	1.233mA/um²
0.1%TTF	7 lots>70yr	6 lots>77yr	4 lots>65yr	4 lots>173yr	3 lots>316yr

Note: Reliability life times are based on listed temperature and used conditions. Detailed WLR test conditions are available upon request.

6.0 ispMACH 4000V/B/C/ZC/ZE Soft Error Rate Data

Soft Error Rate (SER) testing is conducted to characterize the sensitivity of EECPLD storage and device registered logic elements to High Energy Neutron and Alpha Particle radiation. Charge induced by the impact of these particles can collect at sensitive nodes in the device, and result in changes in the internal electrical states of the device. While these changes do not cause physical damage to the device, they can cause a logical error in device operation.

All testing conforms to JEDEC JESD-89.

Table 6.1 ispMACH 4000 MEASURED FITs / Mb

Stress / Structure	REGISTERED LOGIC	EECLPD
Neutron	0.6	0
Alpha	N/A	0

Note: Detailed SER data is available upon request.

7.0 ispMACH 4000 PACKAGE ASSEMBLY INTEGRITY TESTS

7.1 Wire Bond Shear Test

This procedure is used to measure the wire bond strength at the ball joints. Thirty bonds from a minimum of five devices were used for Wire Bond Shear.

WIRE BOND SHEAR TEST RESULTS: All observations > 15 grams for TQFP and fTBGA.

The average measured bond shear results for TQFP were Cpk of > 3.7 and Ppk of > 3.7.
The average measured bond shear results for 256 ball ftBGA were Cpk of > 3.5 and Ppk of > 3.5

7.2 Wire Bond Pull

This procedure is used to measure the wire bond strength at the ball joints and stitch bonds.
For products evaluation thirty bonds from a minimum of five devices were used for and Wire Bond Pull. Test conditions for these tests were 6 grams minimum for 1.0 mil gold wire

WIRE BOND PULL RESULTS: All observations >6 grams for TQFP and ftbGA packages tested.

The average measured wire bond pull results for TQFP were Cpk of > 2.0 and Ppk of > 2.1.
The average measured wire bond pull results for 256 ball ftBGA were Cpk of > 2.4 and Ppk of > 2.4.

7.3 Solderability

This procedure is used to evaluate the solderability of device terminals normally joined by a soldering operation. An accelerated aging test is included in this test method, which simulates natural aging under a combination of various storage conditions that have deleterious effects. Units are exposed to a 8 hour steam preconditioning followed a flux exposure for 7 seconds and a dip in Pb-free solder alloy @ 245 °C ± 5°C for 5 seconds. Minimum of 22 leads from 3 devices per lot were tested with zero failure acceptance.

No failures were observed for ispMACH 4000 devices in TQFP packages. All the tested units passed. There was less than 5% pitting and dewetting on the solder covered area.

7.4 Physical Dimensions

Devices were measured using the appropriate Lattice Semiconductor case outline drawings.

The 10 devices of TQFP from 3 different lots were measured with no failures found. The calculated Cpk on this small sample is Cpk > 9.6.

The 10 devices 256 ftBGA from 3 different lots were measured with no failures found. The calculated Cpk on this small sample is Cpk > 2.0.

7.5 Solder Ball Shear

For the 256 ball ftBGA ten devices from three lots were tested. All units were exposed to two surface mount reflow simulations. The 256 ball ftBGA package use a 0.40 mm barrier metal diameter. All ball shear observations were > 800 grams. The average measured ball shear results for 256 ball ftBGA packages post reflow stress were Cpk of >2.0.

Note: Mach4K 256 ftBGA packages are qualified by extension from MachXO and ispLSI devices.

8.0 ispMACH 4000 ADDITIONAL FAMILY DATA

Table 8.1: ispMACH 4000 Package Assembly Data – csBGA/ ftBGA

Package Attributes / Assembly Sites	ASEM	Amkor	UNISEM	UTAC
Die Family (Product Line)	ispMACH 4000	ispMACH 4000	ispMACH 4000	ispMACH 4000
Fabrication Process Technology	EE9 (180nm CMOS)	EE9 (180nm CMOS)	EE9 (180nm CMOS)	EE9 (180nm CMOS)
Package Assemble Site	Malaysia	Philippines	Singapore	Singapore
Package Type	csBGA/ucBGA/ ftBGA	csBGA/caBGA/ ftBGA	csBGA	csBGA/ftBGA
Ball Counts	56/64/132/144/ 256	56/132/256/324	56/132	56/132/256
Die Preparation/ Singulation	wafer saw, full cut	wafer saw, full cut	wafer saw, full cut	wafer saw, full cut
Die Attach Material	Ablebond 2100 Series	Ablebond 2300 Series	Ablebond 2100 Series	Ablebond 2300 Series
Mold Compound Supplier/ID	Sumitomo / G770 Series	Sumitomo / G770 Series	Sumitomo / G760 Series	Sumitomo / G770 Series
Wire Bond Material	Gold (Au)	Gold (Au)	Gold (Au)	Gold (Au)
Wire Bond Methods	Thermosonic Ball	Thermosonic Ball	Thermosonic Ball	Thermosonic Ball
Substrate Material	Bismaleimide Triazine HL83X Series	Bismaleimide Triazine HL83X Series	Bismaleimide Triazine HL83X Series	Bismaleimide Triazine HL83X Series
L/F Plating or BGA Ball	Sn96.5/Ag3.0/ Cu0.5	Sn95.5/Ag4.0/ Cu0.5	Sn96.5/Ag3.0/ Cu0.5	Sn95.5/Ag4.0/ Cu0.5
Lead Finish	SnAgCu solder ball	SnAgCu solder ball	SnAgCu solder ball	SnAgCu solder ball
Marking	Laser	Laser	Laser	Laser

Table 8.2: ispMACH 4000 Package Assembly Data – Au-Wire TQFP

Package Attributes / Assembly Sites	ASEM	Amkor	UNISEM	UTAC
Die Family (Product Line)	ispMACH 4000	ispMACH 4000	ispMACH 4000	ispMACH 4000ZE
Fabrication Process Technology	EE9 (180nm CMOS)	EE9 (180nm CMOS)	EE9 (180nm CMOS)	EE9 (180nm CMOS)
Package Assembly Site	Malaysia	Korea	Singapore	Singapore
Package Type	TQFP	TQFP	TQFP	TQFP
Pin Count	44/48/100/144/176	44/48/100/144/176	44/48/100/128/144	100/144
Die Preparation/ Singulation	wafer saw, full cut	wafer saw, full cut	wafer saw, full cut	wafer saw, full cut
Die Attach Material	Ablebond 3230	Ablebond 3230	CRM1076NS	Ablebond 3230
Mold Compound Supplier/ID	Hitachi 9220HF Series	KTMC 5700TQ Series	Sumitomo G700 Series	CEL9510HF10-U
Wire Bond Material	Gold (Au)	Gold (Au)	Gold (Au)	0.8mil Gold (Au)
Wire Bond Methods	Thermosonic Ball	Thermosonic Ball	Thermosonic Bball	Thermosonic Bball
Lead frame Material	Cu Alloy	Cu Alloy	Cu Alloy	Cu Alloy
Lead Finish	Matte Sn (annealed)	Matte Sn (annealed)	Matte Sn (annealed)	Matte Sn (annealed)
Marking	Laser	Laser	Laser	Laser

Table 8.3: ispMACH 4000 Package Assembly Data – Cu-Wire TQFP

Package Attributes / Assembly Sites	UTAC
Die Family (Product Line)	ispMACH 4000ZE
Fabrication Process Technology	EE9 (180nm CMOS)
Package Assembly Site	Singapore
Package Type	TQFP
Pin Count	100/144
Die Preparation/ Singulation	wafer saw, full cut
Die Attach Material	Ablebond 3230
Mold Compound Supplier/ID	CEL8240HF10G
Wire Bond Material	0.8mil Copper (Cu)
Wire Bond Methods	Thermosonic Bball
Lead frame Material	Cu Alloy
Lead Finish	Matte Sn (annealed)
Marking	Laser

9.0 Revision History

Table 9.1: Lattice ispMACH 4000 V/B/C/ZC/ZE Product Family Qualification Summary revisions

Date	Revision	Section	Change Summary
July 2003	A	---	Initial document release.
July 2008	B	3.1 HTOL & 4.0 Package	Added Seiko LC4032ZE & LC4064ZE qual data to this Product Family Qual Summary
August 2009	C	Whole document	New qualification summary reporting format. Also added UMC and Seiko foundry WLR; SER data; ESD/LU; and Package assembly integrity & BOM
May 2011	D	3.4 ESD/LU	Updated Seiko LC4064ZE HBM-ESD data
July 2011	E	3.1 HTOL	Added UMC LC4032ZE & LC4064ZE ELFR data
November 2011	F	4.0 Package Qual Data	Added UTAC package qual for LC4000ZE: TN144 bill-of-materials includes 0.8mil Gold (Au) bond wires; and TCN144 bill-of-materials includes 0.8mil Copper (Cu) bond wires.
October 2012	G	3.4 ESD/LU	Added UMC LC4128ZE HBM, CDM & LU data

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