Lattice Platform Manager Product Family Qualification Summary

Lattice Document # 25 – 106877 November 2015

Dear Customer,

Enclosed is Lattice Semiconductor's Platform Manager Product Family Qualification Report.

This report was created to assist you in the decision making process of selecting and using our products. The information contained in this report represents the entire qualification effort for this device family.

The information is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

Your feedback is valuable to Lattice. If you have suggestions to improve this report, or the data included, we encourage you to contact your Lattice representative.

Sincerely,

James M. Orr
Vice President,
Corporate Quality
Lattice Semiconductor Corporation

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1.0 INTRODUCTION

The Lattice Platform Manager integrates board power management (hot-swap, sequencing, monitoring, reset generation, trimming and margining) and digital board management functions (reset tree, non-volatile error logging, glue logic, board digital signal monitoring and control, system bus interface, etc.) into a single integrated solution.

Power management functions are integrated into a power manager section of the product and digital board management functions are primarily integrated into an FPGA section. The two sections are combined in a single package, integrated solution. The function of the power management section is designed using the LogiBuilder tool provided in Lattice's PAC-Designer® software design tool. The FPGA section can also be designed using the same easy to use software tool. For more complex digital design implementation, the FPGA section designs can also be implemented in VHDL or Verilog HDL using Lattice's ispLEVER® software design tool.

The Platform Manager product family combines two proven die solutions into both a stacked die TQFP and a multi-chip module ftBGA package configurations. The power management section is comprised of an ispPAC-POWR1220AT8 die, which is built on the EE8A process technology. EE8A is a 0.35um Electrically Erasable (E2 cell based) CMOS process at United Microelectronics Company (UMC). The FPGA section of a Platform Manager device is a MachXO640 die, which is built on CS90F (also known as EE12) process technology. CS90F is a 130 nm Flash CMOS process with low-k dielectric and copper metallization, fabricated by Fujitsu Limited. The Platform Manager is assembled at Advance Semiconductor Engineering Kaohsiung, Taiwan (ASET).

The following table shows the functional resources of both the power management and FPGA sections that make up a single-package Platform Manager device.

Table 1.0.1 Lattice Platform Manager Product Family Attributes

Parameter	LPTM-1247	LPTM-12107
Analog Inputs	12	12
Margin & Trim	6	8
Total I/O	47	107
CPLD Macrocells	48	48
FPGA LUTs	640	640
Package	128-pin TQFP	208-ball ftBGA

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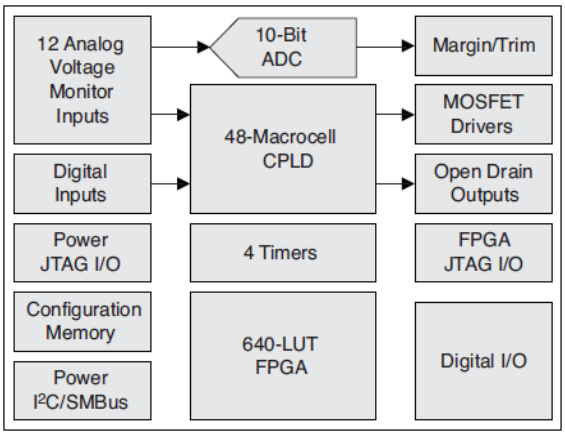
The following block diagram shows how the power management section (with its own 48-Macrocell CPLD) and FPGA section (with a 640-LUT) relate to each other within each Platform Manager device.

Figure 1.0.2 Lattice Platform Manager Block Diagram



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2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office or downloaded from the lattice website at www.latticesemi.com. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8-Discipline (8D) process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITS. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Table 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at www.latticesemi.com/lit/docs/qa/product_reliability_monitor.pdf.

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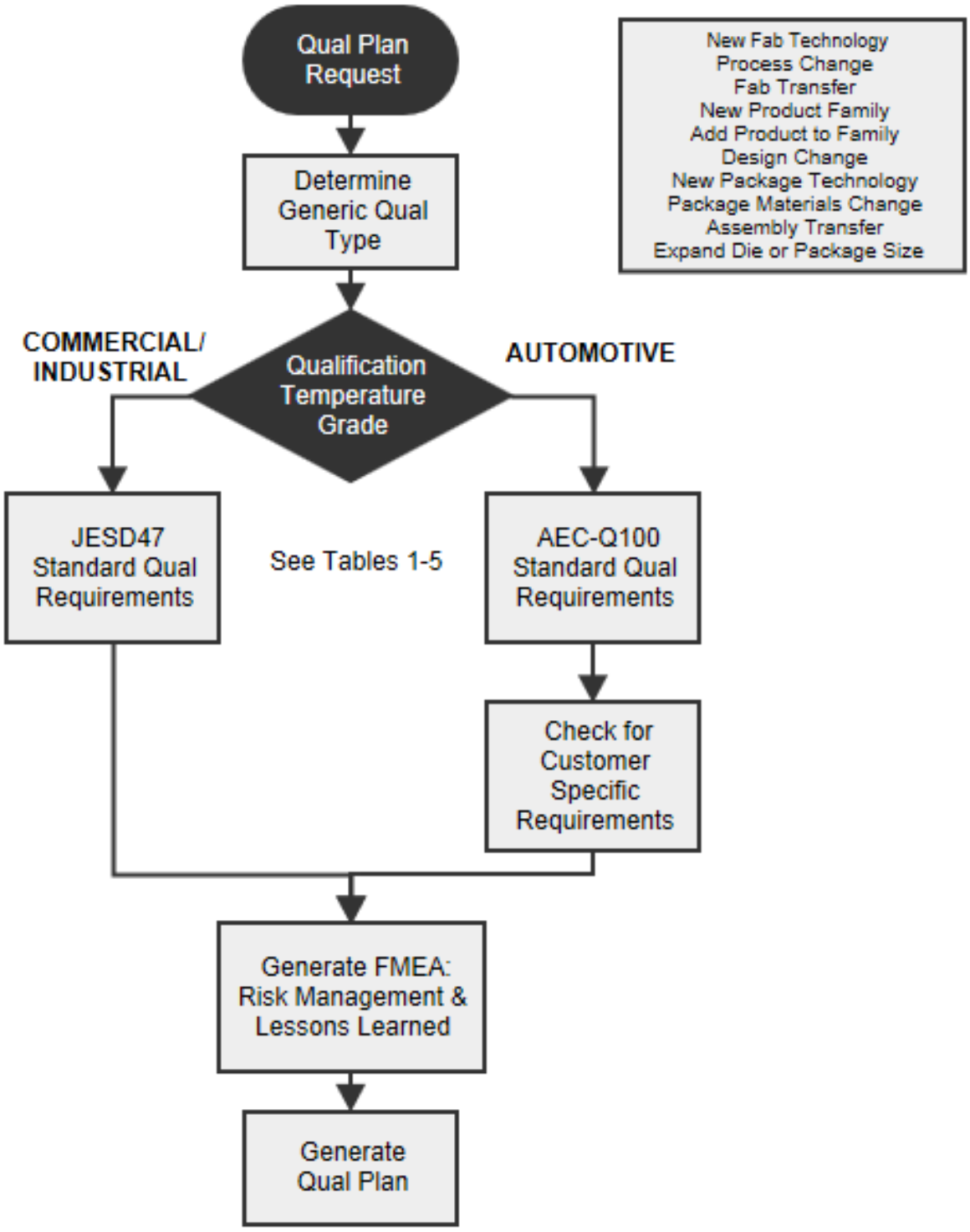
Figure 2.0.1 Platform Manager Product Qualification Process Flow



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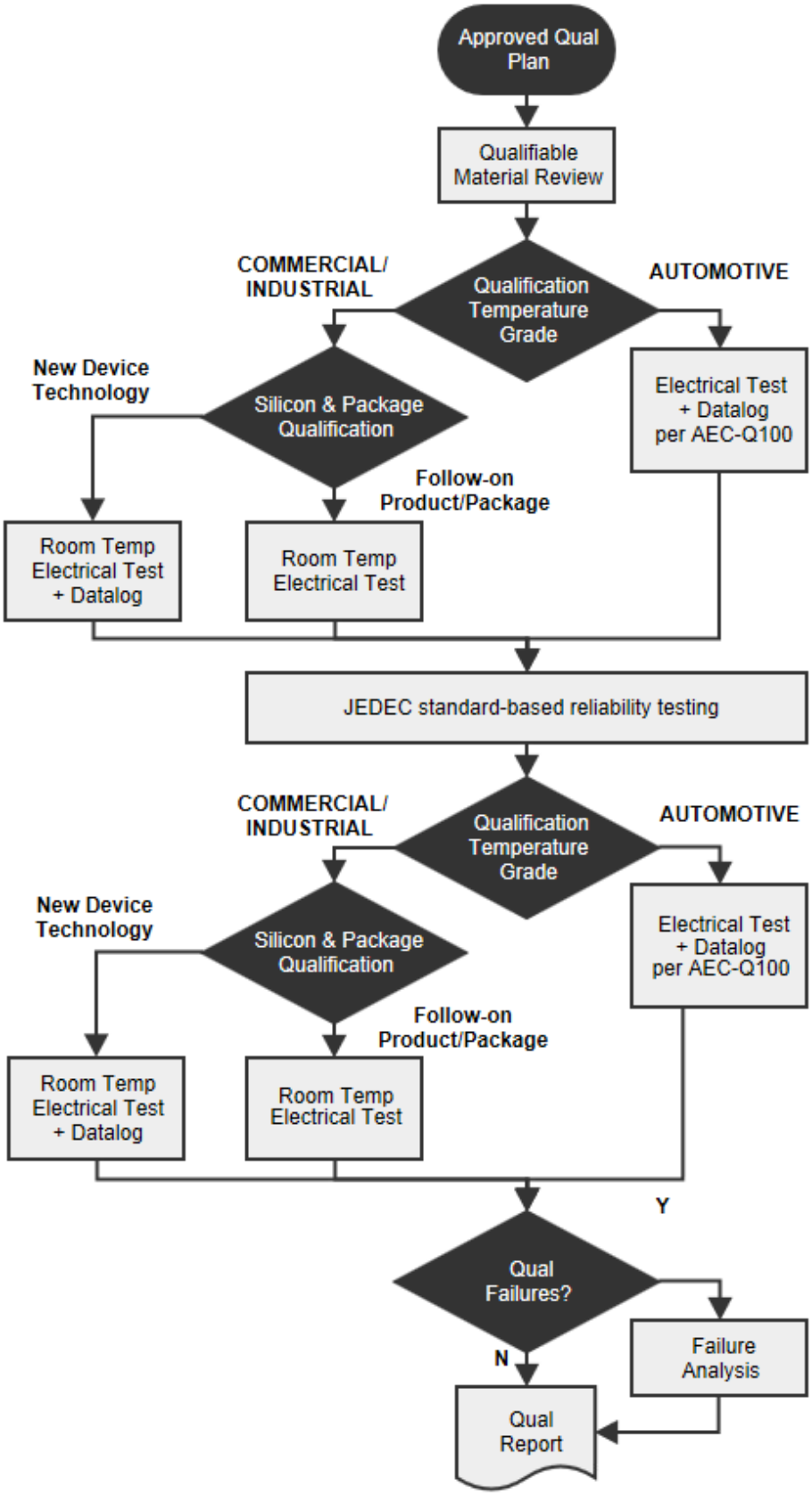

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Table 2.0.2 Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typical)	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 87-101943, MIL-STD-883, Method 1005.8, JESD22-A108 LatticeECP3	125°C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs	77 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification
High Temp Storage Life HTSL	Lattice Procedure # 87-101925, JESD22-A103 LatticeECP3	150°C, at 168, 500, 1000, 2000 hours	77 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification
ESD HBM	Lattice Procedure # 70-100844, MIL-STD-883, Method 3015.7 JESD22-A114	Human Body Model	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD MM	JESD22-A115	Machine Model (MM) sweep to 200 volts	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD CDM	Lattice Procedure # 70-100844, JESD22-C101	Charged Device model	3 parts/lot 1-2 lots typical	Design, Foundry Process
Latch Up Resistance LU	Lattice Procedure # 70-101570, JESD78	±100 ma on I/O's, Vcc +50% on Power Supplies. (Max operating temp.)	6 parts/lot 1-2 lots typical	Design, Foundry Process
Surface Mount Pre-conditioning SMPC	Lattice Procedure # 70-103467, IPC/JEDEC J-STD-020D.1 JESD-A113 FPGA - MSL 3	10 Temp cycles, 24 hr 125°C Bake 192hr. 30/60 Soak 3 SMT simulation cycles	All units going into Temp Cycling, UHAST, BHAST, 85/85	Plastic Packages only
Temperature Cycling TC	Lattice Procedure #70-101568, MIL-STD- 883, Method 1010, Condition B JESD22-A104	(1000 cycles) Repeatedly cycled between -55°C and +125° C in an air environment	77 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification
Unbiased HAST UHAST	Lattice Procedure # 70-104285 JESD22-A118	2 atm. Pressure, 96 hrs, 130°C, 85% Relative Humidity	77 parts/lot 2-3 lots	Foundry Process, Package Qualification Plastic Packages only
Temperature Humidity Bias, THB 85/85, or Biased HAST BHAST (condition A or B)	JESD22-A101 85/85 Or, JESD22-A110 BHAST	Biased to Vcc-maximum plus: 85°C, 85% RH, 1000 hours. Condition A = 96 hrs, 130°C, 85% Relative Humidity. Or, Condition B = 264 hrs, 110°C, 85% Relative Humidity.	77 parts/lot 2-3 lots	Package Qualification

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3.0 SILICON QUALIFICATION DATA FOR THE PLATFORM MANAGER PRODUCT FAMILY

The Platform Manager product family combines two proven die solutions into both a stacked die TQFP and a multi-chip module ftBGA package configurations. The power management section is comprised of an ispPAC-POWR1220AT8 die, which is built on the EE8A process technology. EE8A is a 0.35um Electrically Erasable (E2 cell based) CMOS process at United Microelectronics Company (UMC). The FPGA section of a Platform Manager device is a MachXO640 die, which is built on CS90F (also known as EE12) process technology. CS90F is a 130 nm Flash CMOS process with low-k dielectric and copper metallization, fabricated by Fujitsu Limited (Mie-323 200mm foundry). Both die going into the Platform Manager product family were previously qualified and are in volume production. Therefore, no additional silicon specific qualification data was generated for this product family. In 2015, POWR1220AT8 and MachXO640 dies from alternate foundry sites, Seiko-Epson at Sakata and Mie-101 300mm (CS90F-K) foundry, respectively, was utilized for the Platform Manager device, each separately qualified. The combined silicon qualifications are shown below.

3.1 CS90F/F-K FPGA & EE8A CPLD Life Test Data (ELFR & HTOL)

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

HTOL Stress Conditions:

Stress Duration: 168, 500, 1000 and 2000 hours
Temperature: 125°C

Stress Voltage POWR1220AT8: V_{CC}=3.6V
Stress Voltage POWR1014A & LA-ispPAC-POWR1014A: V_{CC}=3.6V
EE8A CPLD's Pre-conditioned with 100 read/write cycles

Stress Voltage LatticeXP: V_{CC}=1.26V/ V_{CCIO}=3.6V, V_{CC}=2.5V/ V_{CCIO}=3.6V
Stress Voltage MachXO & LAMachXO: V_{CC}=1.3V (E) or 3.6V (C) / V_{CCIO}=3.6V
CS90F/F-K FPGA's Pre-conditioned with 1000 read/write cycles

Method: Lattice Document # 87-101943 and JESD22-A108

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Table 3.1.1 CS90F/F-K and EE8A HTOL Results

Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	1500 Hrs Result	2000 Hrs Result	Cumulative Hours
LA-ispPAC-POWR1014A	Epson	Lot #11	77	N/A	0	N/A	N/A	N/A	38,500
LA-ispPAC-POWR1014A	Epson	Lot #12	77	N/A	0	N/A	N/A	N/A	38,500
ispPAC-POWR1220AT8	Epson	Lot #1	77	0	0	0	N/A	N/A	77,000
ispPAC-POWR1220AT8	Epson	Lot #2	77	0	0	0	N/A	N/A	77,000
ispPAC-POWR1220AT8	Epson	Lot #3	77	0	0	0	N/A	N/A	77,000
ispPAC-POWR1220AT8	Epson	Lot #4	26	0	0	0	N/A	N/A	26,000
ispPAC-POWR1220AT8	Epson	Lot #5	26	0	0	0	N/A	N/A	26,000
ispPAC-POWR1220AT8	Epson	Lot #6	26	0	0	0	N/A	N/A	26,000
ispPAC-POWR1220AT8	Epson	Lot #7	26	N/A	N/A	0	0	0	26,000
ispPAC-POWR1220AT8	UMC	Lot #1	75	0	0	0	0	0	150,000
ispPAC-POWR1220AT8	UMC	Lot #2	77	0	0	0	0	0	154,000
ispPAC-POWR1014A	UMC	Lot #1	78	0	0	0	0	0	156,000
ispPAC-POWR1014A	UMC	Lot #2	78	0	0	0	0	0	156,000
LA-ispPAC-POWR1014A	UMC	Lot #1	76	0	0	0	N/A	N/A	76,000
LA-ispPAC-POWR1014A	UMC	Lot #5	77	0	0	0	N/A	N/A	77,000
LA-ispPAC-POWR1014A	UMC	Lot #7	77	0	N/A	N/A	N/A	N/A	12,936
LA-ispPAC-POWR1014A	UMC	Lot #8	77	0	0	0	N/A	N/A	77,000
LA-ispPAC-POWR1014A	UMC	Lot #9	75	0	0	0	N/A	N/A	75,000
LA-ispPAC-POWR1014A	UMC	Lot #10	77	0	0	0	N/A	N/A	77,000
LCMXO2280C	Mie-101	Lot #1	78	0	NA	NA	NA	NA	13,104
LCMXO2280E	Mie-101	Lot #1	84	0	0	0	NA	NA	84,000
LCMXO2280E	Mie-101	Lot #2	85	0	0	0	NA	NA	85,000
LCMXO2280E	Mie-101	Lot #3	85	0	0	0	NA	NA	85,000
LCMXO640E	Mie-323	Lot #1	44	0	0	0	0	0	88,000
LCMXO640C	Mie-323	Lot #1	44	0	0	0	0	0	88,000
LCMXO640E	Mie-323	Lot #2	44	0	0	0	0	0	88,000
LCMXO640C	Mie-323	Lot #2	44	0	0	0	0	0	88,000
LCMXO640E	Mie-323	Lot #3	40	0	0	0	0	0	80,000
LCMXO640C	Mie-323	Lot #3	40	0	0	0	0	0	80,000
LCMXO256E	Mie-323	Lot #1	38	0	0	0	0	0	76,000
LCMXO256C	Mie-323	Lot #1	38	0	0	0	0	0	76,000
LCMXO256E	Mie-323	Lot #2	38	0	0	0	0	0	76,000
LCMXO256C	Mie-323	Lot #2	38	0	0	0	0	0	76,000
LFXP10C	Mie-323	Lot #A	70	0	0	0	N/A	N/A	70,000
LFXP10C	Mie-323	Lot #B	50	0	0	0	0	0	100,000
LFXP10C	Mie-323	Lot #C	75	0	0	0	0	0	150,000
LFXP10E	Mie-323	Lot #D	59	0	0	0	0	N/A	88,500
LFXP10E	Mie-323	Lot #E	35	0	0	0	0	0	70,000
LFXP3E	Mie-323	Lot #1	76	0	0	0	0	0	152,000
LFXP3E	Mie-323	Lot #2	75	0	0	0	0	0	150,000

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Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	1500 Hrs Result	2000 Hrs Result	Cumulative Hours
LAMXO256C	Mie-323	Lot #9	79	0	0	0	N/A	N/A	79,000
LAMXO256E	Mie-323	Lot# 10	78	0	0	0	N/A	N/A	78,000
LAMXO640E	Mie-323	Lot #12	80	0	0	0	N/A	N/A	80,000

CS90F/F-K Cumulative Device Hours = 2,100,604
CS90F/F-K Cumulative Sample Size = 0 / 1,417
CS90F/F-K FIT Rate = 8 FIT

EE8A Cumulative Device Hours = 1,422,936
EE8A Cumulative Sample Size = 0 / 1256
EE8A FIT Rate = 9 FIT

Platform Manager combined FIT rate: 17FIT

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Early Life Failure Rate (ELFR) Test

The Early Life Failure Rate (ELFR) evaluation is generated using the High Temperature Operating Life test conditions to verify device quality. ELFR is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at maximum Vcc/Vvcio.

ELFR Stress Conditions:

Stress Duration: 24 or 48 hours
Temperature: 125°C

Stress Voltage LA-ispPAC-POWR1014A: V_{CC}=3.6V
EE8A CPLD's Preconditioned with 100 read/write cycles

Stress Voltage LAMachXO: V_{CC}=1.3V (E) or 3.6V (C) / V_{CCIO}=3.6V
CS90F FPGA's Preconditioned with 1000 read/write cycles

Method: Lattice Document # 87-101943 and JESD22-A108

Table 3.1.2 CS90F and EE8A ELFR Results

Product Name	Foundry	Lot #	Qty	24 Hrs Result	48 Hrs Result
LA-ispPAC-POWR1014A	UMC	Lot #1	799	0	N/A
LA-ispPAC-POWR1014A	UMC	Lot #5	797	0	N/A
LA-ispPAC-POWR1014A	UMC	Lot #7	813	0	N/A
LAMXO256C	Mie-323	Lot #9	555	N/A	0
LAMXO256E	Mie-323	Lot #10	786	N/A	0
LAMXO640E	Mie-323	Lot #11	387	N/A	0
LAMXO640E	Mie-323	Lot #12	714	N/A	0

C90F ELFR Cumulative Results = 0 / 2,442

EE8A ELFR Cumulative Results = 0 / 2,486

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3.2 CS90F/F-K FPGA & EE8A CPLD NVM High Temperature Data Retention (HTRX)

High Temperature Data Retention (HTRX)

The High Temperature Data Retention test measures the reliability of Non-Volatile Memory cells while the High Temperature Operating Life test is structured to measure functional operating circuitry failure mechanisms. The CPLD utilizes an Electrically Erasable (E2) NVM cell, while the FPGA utilizes a Flash NVM cell. The High Temperature Data Retention test is specifically designed to accelerate charge gain on to or charge loss off of the NVM cells in the array. Since the charge on these cells determines the actual pattern and function of the device, this test is a measure of the reliability of the device in retaining programmed information. In High Temperature Data Retention, the NVM cell reliability is determined by monitoring the cell margin after biased static operation at 150°C. All cells in all arrays are life tested in both programmed and erased states.

Data Retention (HTRX) Conditions:

Stress Duration: 168, 500, 1000 hours
Temperature: 150°C

Stress Voltage POWR1220AT8: V_{CC}=3.6V
Stress Voltage LA-ispPAC-POWR1014A: V_{CC}=3.6V
EE8A CPLD's Preconditioned with 100 read/write cycles

Stress Voltage MachXO & LAMachXO: V_{CC}=1.3V (E) or 3.6V (C) / V_{CCIO}=3.6V
Stress Voltage LatticeXP: V_{CC}=1.26V/ V_{CCIO}=3.6V, V_{CC}=2.5V/ V_{CCIO}=3.6V
CS90F/F-K FPGA's Preconditioned with 1000 read/write cycles

Method: Lattice Document # 87-101925 and JESD22-A103 / JESD22-A117

Table 3.2.1 CS90F/F-K and EE8A High Temperature Data Retention Results

Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
LA-ispPAC-POWR1014A	Epson	Lot #11	78	0	0	N/A	N/A	39,000
LA-ispPAC-POWR1014A	Epson	Lot #13[A]	39	N/A	0	N/A	N/A	19,500
LA-ispPAC-POWR1014A	Epson	Lot #14[B]	39	N/A	0	N/A	N/A	19,500
ispPAC-POWR1220AT8	Epson	Lot #1	26	0	0	0	N/A	26,000
ispPAC-POWR1220AT8	Epson	Lot #2	77	0	0	0	N/A	77,000
ispPAC-POWR1220AT8	Epson	Lot #3	77	0	0	0	N/A	77,000
ispPAC-POWR1220AT8	Epson	Lot #8[A]	26	0	0	0	N/A	26,000
ispPAC-POWR1220AT8	Epson	Lot #9[B]	26	0	0	0	N/A	26,000
POWR1220AT8	UMC	Lot #1	100	N/A	0	0	N/A	100,000
POWR1220AT8	UMC	Lot #2	100	N/A	0	0	N/A	100,000
LA-ispPAC-POWR1014A	UMC	Lot #1	77	0	0	0	N/A	77,000
LA-ispPAC-POWR1014A	UMC	Lot #2	77	0	0	0	N/A	77,000
LA-ispPAC-POWR1014A	UMC	Lot #3	77	0	0	0	N/A	77,000

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Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
LCMXO2280C	Mie-101	Lot #1*	28	0	0	0	NA	28,000
LCMXO2280C	Mie-101	Lot #2*	28	0	0	0	NA	28,000
LCMXO2280C	Mie-101	Lot #3*	28	0	0	0	NA	28,000
LCMXO2280E	Mie-101	Lot #1*	27	0	0	0	NA	27,000
LCMXO2280E	Mie-101	Lot #2*	27	0	0	0	NA	27,000
LCMXO2280E	Mie-101	Lot #3*	27	0	0	0	NA	27,000
LCMXO640C	Mie-323	Lot #1	88	0	0	0	N/A	88,000
LCMXO640C	Mie-323	Lot #2	88	0	0	0	N/A	88,000
LAMXO256C	Mie-323	Lot #9	80	0	0	0	N/A	80,000
LAMXO256E	Mie-323	Lot# 10	80	0	0	0	N/A	80,000
LAMXO640E	Mie-323	Lot #12	78	0	0	0	N/A	78,000
LFXP10C	Mie-323	Lot #3	148	0	0	0	0	296,000
LFXP10C	Mie-323	Lot #6	150	0	0	0	0	300,000
LFXP10C	Mie-323	Lot #7	55	0	0	0	0	110,000

* These lots have copper (Cu) wire bonds & stressed as High Temperature Storage Life (150°C bake – NVM cells erased).
A: Lot #8 and #13 is a thin tunnel oxide process split.
B: Lot #9 and #14 is a thick tunnel oxide process split.

C90F/F-K Cumulative HTRX Device Hours = 1,285,000
CS90F/F-K Cumulative HTRX Failure Rate = 0 / 932

EE8A Cumulative HTRX Device Hours = 741,000
EE8A Cumulative HTRX Failure Rate = 0 / 819

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3.3 CS90F/F-K FPGA & EE8A CPLD NVM Extended Endurance Cycling

Extended Endurance Cycling (ExtEnd) testing measures the durability of the Non-Volatile Memories (NVM) through program and erase cycles. Endurance testing consists of repeatedly programming and erasing all cells in the array at 25°C to simulate the programming cycles that the user would perform. This test evaluates the integrity of the tunnel oxide through which current passes to program and erase the NVM cells. The CPLD utilizes an Electrically Erasable (E2) NVM cell, while the FPGA utilizes a Flash NVM cell.

NVM ExtEnd Test Conditions:

Stress Duration: 1K, 2K, 3K, 5K, 10K Cycles
Temperature: 150°C

Stress Voltage MachXO (LCMXO): V_{CC}=3.6V/ V_{CCIO}=3.6V
Stress Voltage LatticeXP (LFXP): V_{CC}=2.5V/ V_{CCIO}=3.6V
Stress Voltage POWR1220AT8: Vcc=3.6V

Method: Lattice Document # 70-104633 and JESD22-A117A

Table 3.3.1 CS90F/F-K and EE8A NVM Extended Endurance Cycling Results

Product Name	Wafer Fab	Lot #	Qty	1K Cycles	2K Cycles	3K Cycles	5K Cycles	10K Cycles	Cumulative Cycles
ispPAC-POWR1220AT8	Epson	Lot #1	10	0	N/A	N/A	N/A	N/A	10,000
ispPAC-POWR1220AT8	Epson	Lot #2	10	0	N/A	N/A	N/A	N/A	10,000
ispPAC-POWR1220AT8	Epson	Lot #3	10	0	N/A	N/A	N/A	N/A	10,000
ispPAC-POWR1220AT8	Epson	Lot #8[A]	10	0	N/A	N/A	N/A	N/A	10,000
ispPAC-POWR1220AT8	Epson	Lot #9[B]	10	0	N/A	N/A	N/A	N/A	10,000
ispPAC-POWR1014A	Epson	Lot #11	10	0	N/A	N/A	N/A	N/A	10,000
ispPAC-POWR1014A	Epson	Lot #13[A]	5	0	N/A	N/A	N/A	N/A	5,000
ispPAC-POWR1014A	Epson	Lot #14[B]	5	0	N/A	N/A	N/A	N/A	5,000
POWR1220AT8	UMC	Lot #3	10	0	0	0	0	0	100,000
LCMXO2280E	Mie-101	Lot #1	79	0	0	0	0	0	790,000
LCMXO640C	Mie-323	Lot #3	24	0	0	0	0	0	240,000
LFXP10C	Mie-323	Lot #6	10	0	0	0	0	0	100,000
LFXP10C	Mie-323	Lot #7	10	0	0	0	0	0	100,000

A: Lot #8 and #13 is a thin tunnel oxide process split.
B: Lot #9 and #14 is a thick tunnel oxide process split.

Cumulative Endurance Cycles = 1,400,000
Cumulative EEFailure Rate = 0 / 203

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3.4 Platform Manager Product Family – ESD and Latch UP Data

Electrostatic Discharge-Human Body Model:

Platform Manager product family was tested per the JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure and Lattice Procedure # 70-100844.
All units were tested at 25°C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.1 Platform Manager ESD-HBM Data

Product	128TQFP	208ftBGA
CPLD + FPGA	>1500V	>1500V

HBM classification for Commercial/Industrial products, per JESD22-A114
All HBM levels indicated are dual-polarity (±).

Electrostatic Discharge-Machine Model:

Platform Manager product family was tested per the JESD22-A115 Electrostatic Discharge (ESD) Sensitivity Testing, Machine Model (MM) procedure.
All units were tested at 25°C and +105°C prior to reliability stress and after reliability stress. No failures were observed within the passing stress level.

Table 3.4.2 Platform Manager ESD-MM Data

Product	128TQFP	208ftBGA*
CPLD + FPGA		>50V
CPLD + FPGA		>100V
CPLD + FPGA		>200V

ESD-MM stress level for Commercial/Industrial products, per JESD22-A115
*ESD-MM stress level was performed at 3 voltages to ensure full coverage

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Electrostatic Discharge-Charged Device Model:

Platform Manager product family was tested per the JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure and Lattice Procedure # 70-100844.

All units were tested at 25°C prior to reliability stress and after reliability stress. No failures were observed within the passing Classification.

Table 3.4.3 Platform Manager ESD-CDM Data

Product	128TQFP	208ftBGA
CPLD + FPGA	>1000V	>1000V

CDM classification for Commercial/Industrial products, per JESD22-C101
All CDM levels indicated are dual-polarity (±).

Latch-Up:

Platform Manager product family was tested per the JEDEC EIA/JESD78 IC Latch-up Test procedure and Lattice Procedure # 70-101570. All Latch-up units are stressed at hot (105°C)

All units were tested at 25°C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.4 Platform Manager I/O Latch Up Data

Product	128TQFP	208ftBGA
CPLD + FPGA	>± 100mA	>± 100mA

I-Test LU classification for Commercial/Industrial products, per JESD78.
All IO-LU levels indicated are dual-polarity (±).

Table 3.4.5 Platform Manager Vcc Latch Up Data

Product	128TQFP	208ftBGA
CPLD + FPGA	>1.5x Vcc	>1.5x Vcc

Vsupply Over-voltage Test LU classification for Commercial/Industrial products, per JESD78.

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4.0 PACKAGE QUALIFICATION DATA FOR THE PLATFORM MANAGER PRODUCT FAMILY

The Platform Manager's pair of die is assembled at Advance Semiconductor Engineering Kaohsiung, Taiwan (ASET), in both stacked die TQFP and multi-chip module ftBGA package configurations.

Product Family: LPTM10-1247-3TG128 & LPTM10-12107-3FTG208

Packages offered: 128 TQFP (stacked die) & 208 ftBGA (multi-chip module)

4.1 Platform Manager Product Family Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JEDEC JESD22-A113 "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

Consistent with Lattice Semiconductor Corp. document # 25-100164, package reliability testing can be qualified by extension. Once a package outline is qualified within a package grouping as per doc #70-103639, all lower lead count (and smaller body size) packages within that package type and assembly technology are qualified by extension. Additionally, once an assembly technology has been qualified for one package type, that package type shall be qualified by extension to all future fabrication processes as long as those processes continue to use the same critical elements. Those critical elements in this case, are that the process-to-process interlayer dielectric material and thickness differences do not exceed the current production process limits for the qualification vehicle used. For 180nm and older technologies, the critical elements are considered equivalent.

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Surface Mount Preconditioning (MSL3): (10 Temperature Cycles between -55°C and 125°C, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, Reflow Simulation, 3 passes) performed before all Platform Manager package tests.

Package Types: 128-TQFP (stacked die) & 208-ftBGA (multi-chip module)

Method: Lattice Procedure # 70-103467, J-STD-020 and JESD22-A113

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #1	332	*1	260°C
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #2	332	0	260°C
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #3	332	0	260°C
LPTM10-1247-3TG128	128-TQFP	ASET	**Lot #1	254	0	260°C
LPTM10-1247-3TG128	128-TQFP	ASET	**Lot #2	255	0	260°C
LPTM10-1247-3TG128	128-TQFP	ASET	**Lot #3	255	0	260°C
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #1	332	0	260°C
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #2	332	0	260°C
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #3	332	0	260°C

* FAR1385: 1 failure for ADC_MUX on the CPLD (a random silicon failure unrelated to the package qualification).
**These qualification lots are assembled from the alternate material set defined in Lattice PCN03A-15

128-TQFP Cumulative SMPC Failure Rate = 1 / 1,760
208-ftBGA Cumulative SMPC Failure Rate = 0 / 996

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4.2 High Temperature Storage Life (HTSL)

High Temperature Storage Life (HTSL) test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms in the die and package. Units were stressed per JESD22-A103, High Temperature Storage Life. The HTSL units were stressed at 150°C. Prior to HTSL testing, all devices are subjected to Surface Mount Preconditioning.

High Temperature Storage Life (HTSL) Stress Conditions:

Stress Duration: 168, 500, 1000, hours

Temperature: 150°C

Package Types: 128-TQFP (stacked die) & 208-ftBGA (multi-chip module)

Method: Lattice Document # 87-101925 and JESD22-A103 / JESD22-A117

Table 4.2.1 High Temperature Storage Life Results

Product Name	Package	Assembly Site	Lot Number	Quantity	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #1	82	0	0	0	82,000
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #2	82	0	0	0	82,000
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #3	82	0	0	0	82,000
LPTM10-1247-3TG128	128-TQFP	ASET	**Lot #1	80	N/A	N/A	0	80,000
LPTM10-1247-3TG128	128-TQFP	ASET	**Lot #2	80	N/A	N/A	0	80,000
LPTM10-1247-3TG128	128-TQFP	ASET	**Lot #3	80	N/A	N/A	0	80,000
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #1	82	0	0	0	82,000
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #2	82	0	0	0	82,000
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #3	82	0	0	0	82,000

**These qualification lots are assembled from the alternate material set defined in Lattice PCN03A-15

Cumulative HTSL Failure Rate = 0 / 732
Cumulative HTSL Device Hours = 0 / 732,000

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4.3 Platform Manager Product Family Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104 "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

Temperature Cycling (T/C) Stress Conditions:

Stress Duration: 1000 cycles

Stress Conditions: Temperature cycling between -55°C to 125°C

Package Types: 128-TQFP (stacked die) & 208-ftBGA (multi-chip module)

Method: Lattice Procedure # 70-101568 and JESD22-A104

Table 4.3.1 Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Quantity	500 Cycles	1000 Cycles
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #1	82	0	0
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #2	82	0	0
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #3	82	0	0
LPTM10-1247-3TG128	128-TQFP	ASET	**Lot #1	80	N/A	0
LPTM10-1247-3TG128	128-TQFP	ASET	**Lot #2	80	N/A	0
LPTM10-1247-3TG128	128-TQFP	ASET	**Lot #3	80	N/A	0
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #1	82	0	0
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #2	82	0	0
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #3	82	0	0

**These qualification lots are assembled from the alternate material set defined in Lattice PCN03A-15

Cumulative Temp Cycle Failure Rate = 0 / 732

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4.4 Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (UHAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent JEDEC JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," the Unbiased HAST conditions are 96 hour exposure at 130°C or 264 hours at 110°C and 85% relative humidity, and 2 atmospheres of pressure. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

UHAST Stress Conditions:

Stress Duration: 96 hours (130°C) or 264 hours (110°C)

Chamber Conditions: 110°C or 130°C and 85% RH

Package Types: 128-TQFP (stacked die) & 208-ftBGA (multi-chip module)

Method: Lattice Procedure # 70-104285 and JESD22-A118

Table 4.4.1 Unbiased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #1	77	0	96 Hrs
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #2	77	0	96 Hrs
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #3	77	0	96 Hrs
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #1	77	0	264 Hrs
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #2	77	0	264 Hrs
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #3	77	0	264 Hrs

Cumulative Unbiased HAST failure Rate = 0 / 462

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4.5 THB: Biased HAST Data

Biased Highly Accelerated Stress Test (BHAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD A110-B "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are with Vcc bias and alternate pin biasing in an ambient of 110°C or 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

BHAST Stress Conditions:

Stress Duration: 96 hours (130°C) or 264 hours (110°C)

Stress Voltage: Vcc/VccIO = 3.47V, 130°C /85%RH (128-TQFP) or 110°C/85%RH (208-ftBGA)

Chamber Conditions: 110°C or 130°C and 85% RH

Package Types: 128-TQFP (stacked die) & 208-ftBGA (multi-chip module)

Method: Lattice Procedure # 70-101571 and JESD22-A101

Table 4.5.1 Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Temp	Stress Duration
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #1	77	0	110°C	264 Hrs
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #2	77	0	110°C	264 Hrs
LPTM10-1247-3TG128	128-TQFP	ASET	Lot #3	77	0	110°C	264 Hrs
LPTM10-1247-3TG128	128-TQFP	ASET	**Lot #1	79	0	130°C	96 Hrs
LPTM10-1247-3TG128	128-TQFP	ASET	**Lot #2	79	0	130°C	96 Hrs
LPTM10-1247-3TG128	128-TQFP	ASET	**Lot #3	79	0	130°C	96 Hrs
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #1	77	0	110°C	264 Hrs
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #2	77	*1	110°C	264 Hrs
LPTM10-12107-3FTG208	208-ftBGA	ASET	Lot #3	77	0	110°C	264 Hrs

* FAR1384: 1 failure for leakage (I_LEAK_14V_OD_HV3) on the CPLD (a random silicon failure unrelated to the package qualification).
**These qualification lots are assembled from the alternate material set defined in Lattice PCN03A-15

Cumulative Biased HAST failure Rate = 1 / 699

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5.0 WAFER FAB PROCESS RELIABILITY

The Platform Manager product family is a two-die solution, in both stacked die TQFP and multi-chip module ftBGA package configurations and is built on two wafer fab technologies. The CPLD die is built on the EE8A process technology. EE8A is a 0.35um Electrically Erasable (E2 cell based) CMOS process at United Microelectronics Company (UMC). The FPGA die is built on CS90F/F-K (also known as EE12) process technology. CS90F/F-K is a 130 nm Flash CMOS process with low-k dielectric and copper metallization, fabricated by Fujitsu Limited. Platform Manager end-of-life is a combination of Wafer Level Reliability (WLR) from both fabs.

Note: Reliability life times are based on listed temperature and used conditions. Detailed WLR test conditions are available upon request.

5.1 EE8A Process Reliability Wafer Level Review

Several key fabrication process related parameters have been identified by the foundry that would affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): SM is not an issue for the EE8A BEOL (etched Al lines, W plug Vias, SiO IMD).

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Table 5.1 Wafer Level Reliability Results for EE8A (0.35 um) Process Technology

HCI

Device	LVN	LVP
deltaIds	-10%	-10%
Celsius	25	25
Vgstress	Vd/2	0
Vds	3.6	-3.6
TTF	5 lots>32yr	1 lot>1e6yr

TDDB

Device	LVN	MIM
Celsius	130	130
Vg	3.3	20
Area	8000um^2	2.25e4um^2
0.1% TTF	1.4e5yr	>1e6yr

VRDB

Device	Psubs	Nwell	Psubs	Nwell	HVG	TunOx
Celsius	130	130	130	130	130	130
Vg	3.6	-3.6	3.6	-3.6	5	3.6
Tox (A)	80	80	150	150	188	92
Area	max EDR	max EDR	max EDR	max EDR	max EDR	max EDR
10yr FIT	<100	100	<100	<100	<100	<100

EML

Layer	M1	M2	M3
Celsius	130	130	130
Delta R	+20%	+20%	+20%
Jmax	1.0mA/um	1.4mA/um	1.4mA/um
0.1% TTF	3 lots>11yr	3 lots>11yr	2 lots>16yr

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5.2 CS90F Process Reliability Wafer Level Review

Several key fabrication process related parameters have been identified by the foundry that would affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. Normal operating conditions are defined in the Electrical Design Rules (EDR). These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence.

Table 5.2 Wafer Level Reliability Results for CS90F (130 nm) Process Technology

HCI

Device	LVN	MVN	HVN	LVP	MVP	HVP
Celsius	25	25	25	25	25	25
	delta Ids	-10%	-10%	-10%	-10%	-10%
Vds	1.32	3.6	5.5	-1.32	-3.6	-3.6
TTF	3 lots>180yr	5 lots>18yr	4 lots>30yr	3 lots>120yr	3 lots>64yr	3 lots>36yr

TDDB

Device	LVN	MVN	HVN	LVP	MVP	HVP
Celsius	125	125	125	125	125	125
Vg	1.32	3.6	10**	-1.32	-3.6	-10
Max Area	0.001cm^2	0.044cm^2	0.00014cm^2	0.001cm^2	0.044cm^2	0.00002cm^2
0.1% TTF	2 lots>23yr	2 lots>25yr	1 lot>10yr	2 lots>50yr	2 lots>900yr	1 lot>10yr

NBTI

Device	LVP	MVP	HVP
delta Ids	-10%	-10%	-10%
Celsius	125	125	125
Vg	-1.32	-3.6	-5.5
TTF	3 lots>124yr	5 lots>47yr	3 lots>200yr

EML

Device	Intermediate	Semi-Global	Global (Top Al)
Celsius	125	125	125
delta R	+20%	+20%	+20%
Jmax	2.1e^{5}A/ cm^2	2.1e^{5}A/ cm^2	1.68A/ cm^2
0.1% TTF	3 lots>57yr	1 lot>137yr	1 lot>89yr

SM

Device	Intermediate
delta R	+10%
Celsius	125
TTF	3 lots>22yr

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6.0 PLATFORM MANAGER ADDITIONAL FAMILY DATA

Table 6.0.1 Package Assembly Data - 128-TQFP (stacked die) & 208-ftBGA (multi-chip module)

Package Attributes / Assembly Sites	ASET	ASET
Die Family (Product Line)	CPLD + FPGA	CPLD + FPGA
Wafer Fabrication Process	EE8A & CS90F	EE8A & CS90F
Package Assembly Site	Kaohsiung	Kaohsiung
Package Type	TQFP	ftBGA
Die Configuration	Stacked Die	Multi-Chip Module
Pin Count	128	208
Die Preparation/Singulation	wafer saw, full cut	wafer saw, full cut
Die Attach Material	FH900 + Si Spacer	Ablestik 2100A
Mold Compound	CEL-9510HFL-U/EME-G631SH	G2250
Wire Bond Material	Gold (Au)	Gold (Au)
Wire Bond Diameter	0.7mil Au bondwire	0.7mil bondwire
Wire Bond Methods	Thermosonic Ball	Thermosonic Ball
Lead frame or Substrate Material	A07881-0 / A07757-0	Green, AUS308, CL832NX
Lead Finish or Solder Balls	Matte Sn (annealed)	SAC 305
Marking	Laser	Laser

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