LatticeXP2 Product Family Qualification Summary

Lattice Document # 25 - 106588 November 2012

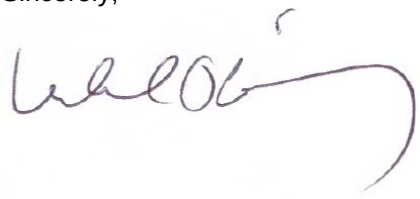
Dear Customer,

Welcome to the Lattice Semiconductor Corp. LatticeXP2 Product Family Qualification Report. This report reflects our continued commitment to product quality and reliability. The information in this report is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

This is the first of a new generation of Product Qualification Summary Reports. The information contained in this document is extensive, and represents the entire qualification effort for this device family. Our goal is to provide this information to support your decision making process, and to facilitate the selection and use of our products.

As always, your feedback is valuable to Lattice. Our goal is to continuously improve our systems, including the generation of this report and the data included. Please feel free to forward your comments and suggestions to your local Lattice representative. We will use that feedback carefully and wisely in our effort to maximize customer satisfaction.

Sincerely,



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INDEX

1.0 INTRODUCTION 4

Table 1.1 LatticeXP2 and LA-LatticeXP2 (Automotive) Product Family Attributes 4

2.0 LATTICE PRODUCT QUALIFICATION PROGRAM 5

Figure 2.1: LFXP2 and LAXP2 (Automotive) Product Qualification Process Flow 6
Table 2.2: Standard Qualification Testing 8

3.0 QUALIFICATION DATA FOR LATTICEXP2 PRODUCT FAMILY 10

3.1 CS100F PRODUCT FAMILY LIFE DATA 10
Table 3.1.1: LatticeXP2 Product Family Life Results 10
3.2 LATTICEXP2 PRODUCT FAMILY HIGH TEMPERATURE RETENTION (HTRX) AND HIGH TEMPERATURE STORAGE LIFE (HTSL) DATA 11
Table 3.2.1: LatticeXP2 High Temperature Retention Results 11
Table 3.2.2: LatticeXP2 High Temperature Storage Life Results 12
3.3 LATTICEXP2 PRODUCT FAMILY FLASH ENDURANCE CYCLING DATA 13
Table 3.3.1: LatticeXP2 Flash Extended Endurance Results 13
3.4 LATTICEXP2 PRODUCT FAMILY – ESD AND LATCH UP DATA 14
Table 3.4.1 LatticeXP2 ESD-HBM Data 14
Table 3.4.2 LFXP2 ESD-MM Data 15
Table 3.4.3 LatticeXP2 ESD-CDM Data 16
Table 3.4.4 LatticeXP2 I/O Latch Up Data 17
Table 3.4.5 LatticeXP2 Vcc Latch Up Data 18

4.0 PACKAGE QUALIFICATION DATA FOR LATTICEXP2 PRODUCT FAMILY 19

Table 4.1 Product-Package Qualification-By-Extension Matrix 19
4.1 LATTICEXP2 PRODUCT FAMILY SURFACE MOUNT PRECONDITIONING TESTING 20
Table 4.1.1 Surface Mount Precondition Data 20
4.2 LATTICEXP2 PRODUCT FAMILY TEMPERATURE CYCLING DATA 22
Table 4.2.1: Temperature Cycling Data 22
4.3 LATTICEXP2 PRODUCT FAMILY UNBIASED HAST DATA 23
Table 4.3.1: Unbiased HAST Data 23
4.4 LATTICEXP2 PRODUCT FAMILY THB: BIASED HAST DATA 24
Table 4.4.1: Biased HAST Data 24

5.0 CS100F PROCESS RELIABILITY WAFER LEVEL REVIEW 25

Table 5.1 – Wafer Level Reliability Results 25

6.0 LATTICEXP2 SOFT ERROR DATA 26

Table 6.1 XP2 MEASURED FITs / Mb 26

7.0 LATTICEXP2 PACKAGE ASSEMBLY INTEGRITY TESTS 27

7.1 WIRE BOND SHEAR TEST 27
7.2 WIRE BOND PULL 27
7.3 SOLDERABILITY 27
7.4 PHYSICAL DIMENSIONS 27
7.5 SOLDER BALL SHEAR 28

8.0 LATTICEXP2 ADDITIONAL FAMILY DATA 29

Table 8.1: LFXP2 and LA-XP2 (Automotive) Package Assembly Data – csBGA/ ftBGA/ fpBGA 29
Table 8.2: LFXP2 and LA-XP2 (Automotive) Package Assembly Data- TQFP. 29

9.0 REVISION HISTORY 30

Table 9.1: LatticeXP2 Product Family Qualification Summary Revisions 30

1.0 INTRODUCTION

The LatticeXP2 and LA-LatticeXP2 (Automotive) devices combine a Look-up Table (LUT)-based FPGA fabric with Flash Non-volatile cells in an architecture referred to as flexiFLASH. The flexiFLASH approach provides benefits such as instant-on, small footprint, on chip storage with FlashBAK embedded block memories and Serial TAG memory and design security. The parts also support Live Updates with TransFR, 128-bit AES Encryption and Dual-Boot technologies. The LatticeXP2 FPGA fabric utilizes an underlying LatticeECP2 architecture that was optimized from the outset with high performance and low cost in mind. The LatticeXP2 devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O and enhanced sysDSP blocks.

The LatticeXP2 product family offers a flexible LUT (Look Up Table) architecture that provides 5K to 40K LUTs and in Chip Scale BGA (csBGA), Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Fine-Pitch Thin BGA (ftBGA) and Fine Pitch BGA (fpBGA) packages with user I/O counts ranging from 86 to 540 I/Os.
The LA-LatticeXP2 product offering provides 5K to 17K LUTs and in Chip Scale BGA (csBGA), Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP) and Fine-Pitch Thin BGA (ftBGA) packages with user I/O counts ranging from 86 to 201 I/Os.

Table 1.1 shows the LUTs, package and I/O options, along with other key parameters.

Table 1.1 LatticeXP2 and LA-LatticeXP2 (Automotive) Product Family Attributes

	LFXP2-5/ LAXP2-5*	**LFXP2-8/ LAXP2-8***	**LFXP2-17/ LAXP2-17***	**LFXP2-30**	**LFXP2-40**
LUTs (K)	5	8	17	29	40
Dist RAM (Kbits)	10	18	35	56	83
EBR SRAM (Kbits)	166	221	276	387	885
EBR SRAM Blocks	9	12	15	21	48
sysDSP Blocks	3	4	5	7	8
18 x 18 Multipliers	12	16	20	28	32
Vcc Voltage	1.2V	1.2V	1.2V	1.2V	1.2V
GPLL	2	2	4	4	4
Max. I/O	172	201	358	472	540
Die Fabrication Site	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie
Fabrication Process Technology	90nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS
Die Size (W x L x T)	4240 x 3930 x 330-381 (um)	4990 x 4770 x 330-381 (um)	6220 x 5950 x 330-381 (um)	7860 x 6950 x 330-381 (um)	8780 x 8310 x 330-381 (um)
Die Metallization	Cu	Cu	Cu	Cu	Cu
Die Interconnect Dielectric	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN
Packages and I/O Combinations					
132-ball csBGA (8x8 mm)*	86	86			
144-pin TQFP (20x20 mm)*	100	100			
208-pin PQFP (28x28 mm)*	146	146	146		
256-ball ftBGA (17x17 mm)*	172	201	201	201	
484-ball fpBGA (23x23 mm)			358	363	363
672-ball fpBGA (27x27 mm)				472	540

* Automotive grade device/packages offered.

The LFXP2 and LA-XP2 devices are implemented on a cost-effective, production-proven, Low-k, 90nm CMOS process with SRAM + FLASH and copper metallization fabricated by Fujitsu Limited. This process technology, combined with efficient silicon design, results in very small die sizes while providing the new Lattice FPGAs with the most attractive feature sets in their class.

INDEX Return

2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8 Discipline (8D) process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITS. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

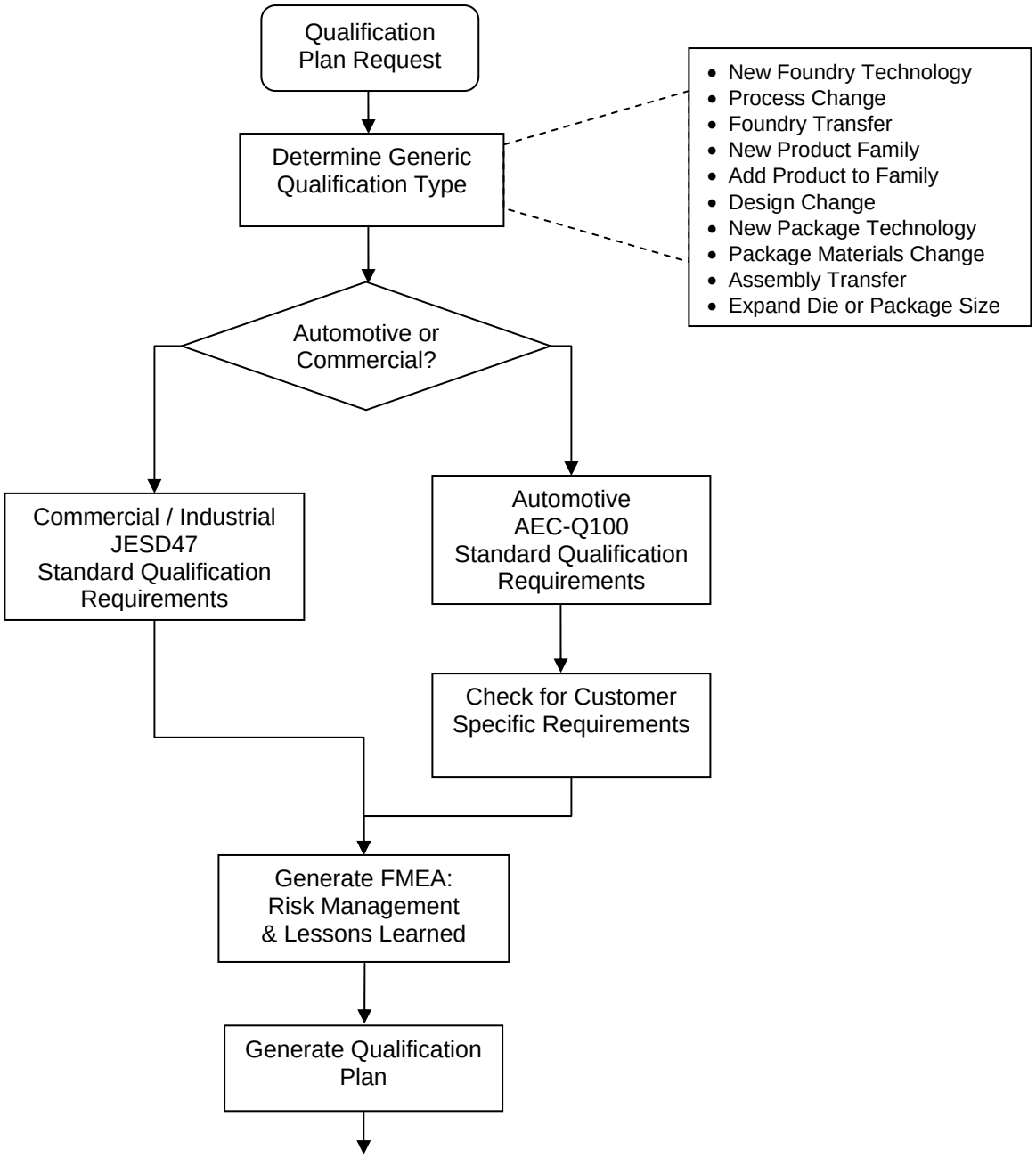
Product families are qualified based upon the requirements outlined in Tables 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The LFXP2 and LAXP2 (Automotive) product family is the Lattice's first Low-k 90nm (a.k.a. CS100F) Flash based Technology product offering and is the primary technology qualification vehicle. This process technology, combined with efficient silicon design, results in very small die sizes.

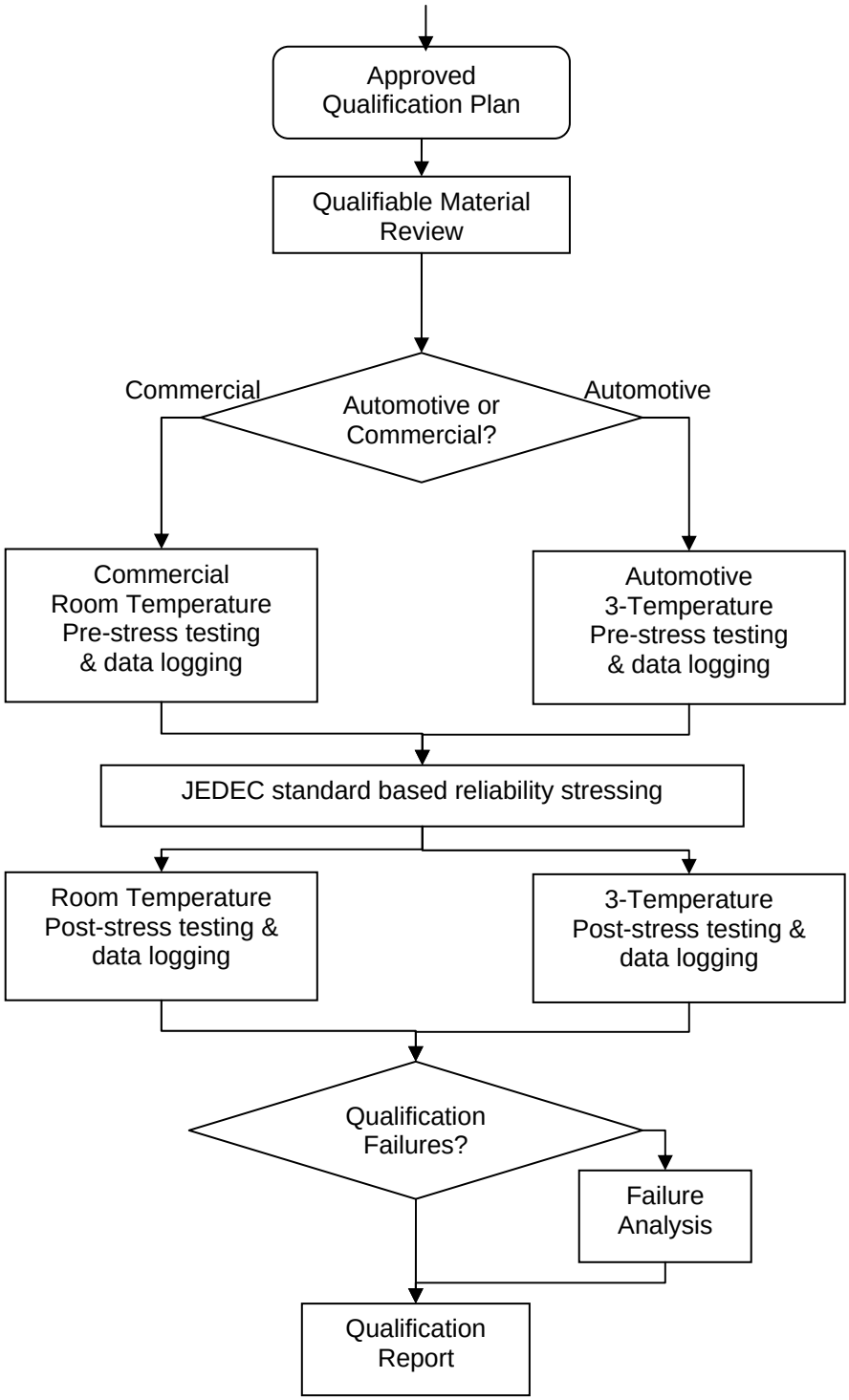
Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at www.latticesemi.com/lit/docs/qa/product_reliability_monitor.pdf .

INDEX Return

Figure 2.1: LFXP2 and LAXP2 (Automotive) Product Qualification Process Flow



INDEX Return



INDEX Return

Table 2.2: Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 87-101943, MIL-STD-883, Method 1005.8, JESD22-A108C LatticeXP2	125° C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs. Preconditioned with 10,000 read/write cycles	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
High Temp Data Retention HTRX	Lattice Procedure # 87-101925, JESD22-A103C JESD22-A117A LatticeXP2	150° C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs. Preconditioned with 10,000 read/write cycles	100/lot 2-3 lots	Design, Foundry Process, Package Qualification E^2 Cell Products Flash based Products
High Temp Storage Life HTSL	Lattice Procedure # 87-101925, JESD22-A103C LatticeXP2	150° C, at 168, 500, 1000, 2000 hours.	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
Endurance - Program/Erase Cycling Flash based Products	Lattice Procedure, # 70-104633 JESD22-A117A LatticeXP2	Program/Erase devices to 100,000 cycles Program/Erase devices to 10X cycles of data sheet specification	10/lot 2-3 lots typical	Design, Foundry Process, Package Qualification
ESD HBM	Lattice Procedure # 70-100844, MIL-STD-883, Method 3015.7 JESD22-A114E	Human Body Model (HBM) sweep to 2000 volts – (130nm and older)	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD MM	JESD22-A115C	Machine Model (MM) sweep to 200 volts	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD CDM	Lattice Procedure # 70-100844, JESD22-C101D	Charged Device model (CDM) sweep to 1000 volts (130nm and older)	3 parts/lot 1-3 lots typical	Design, Foundry Process
Latch Up Resistance LU	Lattice Procedure # 70-101570, JESD78A	±100 ma on I/O's, Vcc +50% on Power Supplies. (Max operating temp.)	6 parts/lot 1-3 lots typical	Design, Foundry Process
Surface Mount Pre-conditioning SMPC	Lattice Procedure # 70-103467, IPC/JEDEC J-STD-020D.1 JESD-A113F CPLD/FPGA - MSL 3	10 Temp cycles, 24 hr 125° C Bake 192hr. 30/60 Soak 3 SMT simulation cycles	All units going into Temp Cycling, UHAST, BHAST, 85/85	Plastic Packages only
Temperature Cycling TC	Lattice Procedure #70-101568, MIL-STD- 883, Method 1010, Condition B JESD22-A104C	(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment	45 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification
Unbiased HAST UHAST	Lattice Procedure # 70-104285 JESD22-A118	2 atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 parts/lot 2-3 lots	Foundry Process, Package Qualification Plastic Packages only

INDEX Return

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
Moisture Resistance Temperature Humidity Bias 85/85 THBS or Biased HAST BHAST	Lattice Procedure # 70-101571, JESD22-A101B JESD22-A110B	Biased to maximum operating Vcc, 85° C, 85% Relative Humidity, 1000 hours or Biased to maximum operating Vcc, 2atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 devices/lot 2-3 lots	Design, Foundry Process, Package Qualification Plastic Packages only
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or applicable LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	Package Qualification
Wire Bond Strength	Lattice Procedure # 70-100220	6 gr. min. for 1.25 mil gold wire	15 devices per pkg. per year	Design, Foundry Process, Package Qualification
Solderability	Lattice Procedure # 70-100212, MIL-STD-883, Method 2003	Steam Pre-conditioning 4-8 hours. Solder dip at 245°C+5°C	22 leads/ 3 devices/ Package family	All packages except BGAs

INDEX Return

3.0 QUALIFICATION DATA FOR LatticeXP2 Product Family

The LatticeXP2 product family is the Lattice's first 90nm (CS100F) Flash Technology based product offering. The LFXP2 and LAXP2 (Automotive) were the primary technology qualification vehicle.

Product Family: **LFXP2, LAXP2**
Packages offered:, csBGA, ftBGA, fpBGA, PQFP and TQFP
Process Technology Node: 90nm

3.1 CS100F Product Family Life Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at VCC 1.26 V/ VCCIO 3.47 V and 125°C ambient. Prior to High Temperature Operating Life testing, all LatticeXP2 and LA-XP2 devices are programmed and erased 10,000 times.

LatticeXP2 Product Family Life Test (HTOL) Conditions:

Stress Duration: 168, 500, 1000 hours.
Temperature: 125°C ambient
Stress Voltage LatticeXP2 (LFXP2, LAXP2): V_{CC}=1.26V/ V_{CCIO}=3.47V
HTOL (1000 hrs) units preconditioned with 10,000 c cycles
ELFR only (48 hrs) units not read/write preconditioned
Method: Lattice Document # 87-101943 and JESD22-A108

Table 3.1.1: LatticeXP2 Product Family Life Results

Product Name	Lot #	Qty	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LAXP2-17E	Lot #8	80	0	0	0	0	80000
LAXP2-17E	Lot #9	95	0	0	0	0	95000
LAXP2-17E	Lot #10	76	0	0	0	0	76000
LFXP2-40E	Lot #1	78		0	0	0	78000
LFXP2-40E	Lot #2	82		0	0	0	82000
LAXP2-5E	Lot #1	822	0				
LAXP2-5E	Lot #2	794	0				
LAXP2-5E	Lot #3	774	0				

CS100F Cumulative Device Hours = 411,000
CS100F Cumulative Sample Size = 0 / 411
CS100F FIT Rate = 29 FIT

LFXP2 Cumulative Result =0 / 160
LAXP2 Cumulative Result = 0 / 251
LAXP2 Cumulative ELFR Result =0 / 2,641

INDEX Return

3.2 LatticeXP2 Product Family High Temperature Retention (HTRX) and High Temperature Storage Life (HTSL) Data

High Temperature Data Retention (HTRX) and High Temperature Storage Life (HTSL)

The High Temperature Data Retention test measures the Flash cell reliability while the High Temperature Operating Life test is structured to measure functional operating circuitry failure mechanisms. The High Temperature Data Retention test is specifically designed to accelerate charge gain on to or charge loss off of the floating gates in the device's array. Since the charge on these gates determines the actual pattern and function of the device, this test is a measure of the reliability of the device in retaining programmed information. In High Temperature Data Retention, the Flash cell reliability is determined by monitoring the cell margin after biased static operation at 150°C ambient. All cells in all arrays are life tested in both programmed and erased states. Prior to data retention testing all products are pre-conditioned to the maximum data sheet conditions program/erase cycles.

LFXP2 and LAXP2 (Automotive) Data Retention (HTRX) Conditions:
Stress Duration: 168, 500, 1000 hours.
Temperature: 150°C ambient
Stress Voltage LatticeXP2 (LFXP2, LAXP2): V_{CC}=1.26V/ V_{CCIO}=3.47V
Method: Lattice Document # 87-101925 and JESD22-A103C / JESD22-A117A

Table 3.2.1: LatticeXP2 High Temperature Retention Results

Product Name	Package	Assembler	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LAXP2-17E	256 ftbGA	ASEM	Lot #8	100	0	0	0	100000
LAXP2-17E	256 ftbGA	ASEM	Lot #9	80	0	0	0	80000
LAXP2-17E	256 ftbGA	ASEM	Lot #10	80	0	0	0	80000
LFXP2-40E	672 fpbGA	ASEM	Lot #1	102	0	0	0	102000

CS100F Cumulative HTRX Failure Rate = 0 / 362
CS100F Cumulative HTRX Device Hours = 362,000

INDEX Return

The High Temperature Storage Life (HTSL) test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms.

LatticeXP2 High Temperature Storage Life (HTSL) Conditions:
Stress Duration: 168, 500, 1000, 1500 hours.
Temperature: 150°C ambient
Method: Lattice Document # 87-101925 and JESD22-A103C / JESD22-A117A

Table 3.2.2: LatticeXP2 High Temperature Storage Life Results

Product Name	Package	Assembler	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LFXP2-17E	256 ftbGA	ASEM	Lot #1	69	0	0	0	69000
LFXP2-5E	144 TQFP	UTAC	Lot #1	77			0	77000
LFXP2-5E	144 TQFP	UTAC	Lot #2	77			0	77000
LFXP2-5E	144 TQFP	UTAC	Lot #3	77			0	77000
LAXP2-8E	256 ftbGA	UTAC	Lot #1	77			0	77000
LAXP2-8E	256 ftbGA	UTAC	Lot #2	77			0	77000
LAXP2-8E	256 ftbGA	UTAC	Lot #3	77			0	77000

CS100F Cumulative HTSL Failure Rate = 0 / 531
CS100F Cumulative HTSL Device Hours = 531,000

INDEX Return

3.3 LatticeXP2 Product Family Flash Endurance Cycling Data

Flash Extended Endurance testing measures the durability of the device through programming and erase cycles. Endurance testing consists of repeatedly programming and erasing all cells in the array at 25°C / 115°C ambient to simulate programming cycles the user would perform. This test evaluates the integrity of the thin tunnel oxide through which current passes to program the floating gate in each cell of the array.

LatticeXP2 Flash Extended Endurance Test Conditions:
Stress Duration: 1K, 2K, 3K, 5K, 10K Cycles
Temperature: 25°C / 115°C ambient
Stress Voltage LatticeXP2 (LFXP2, LAXP2): V_{CC}=1.26V/ V_{CCIO}=3.47V
Method: Lattice Document # 70-104633 and JESD22-A117A

Table 3.3.1: LatticeXP2 Flash Extended Endurance Results

Product Name	Lot #	Qty	#Flash Cells	Cycling Temp	1k CYC	10k CYC	20k CYC	50k CYC	100k CYC	Post Cycling Stress	Cumulative Flash Cells Prgm/Erase Cycles
LFXP2-17E	Lot #1	10	4.E+06	115C	0					ExtEnd	3.636E+10
LFXP2-17E	Lot #3	10	4.E+06	115C	0					ExtEnd	3.636E+10
LAXP2-17E	Lot #8	80	4.E+06	25C		0				HTOL	2.909E+12
LAXP2-17E	Lot #9	95	4.E+06	25C		0				HTOL	3.454E+12
LAXP2-17E	Lot #10	76	4.E+06	25C		0				HTOL	2.763E+12
LAXP2-17E	Lot #8	100	4.E+06	25C		0				HTRX	3.636E+12
LAXP2-17E	Lot #9	80	4.E+06	25C		0				HTRX	2.909E+12
LAXP2-17E	Lot #10	80	4.E+06	25C		0				HTRX	2.909E+12
LFXP2-17E	Lot #3	10	8.E+06	25C			0			ExtEnd	1.661E+12
LFXP2-17E	Lot #3	10	8.E+06	25C				0		ExtEnd	4.152E+12
LFXP2-17E	Lot #3	10	8.E+06	25C					0	ExtEnd	8.304E+12
LFXP2-40E	Lot #1	78	8.E+06	25C		0				HTOL	6.477E+12
LFXP2-40E	Lot #2	82	8.E+06	25C		0				HTOL	6.809E+12
LFXP2-40E	Lot #1	102	8.E+06	25C		0				HTRX	8.470E+12
LFXP2-40E	Lot #1	30	8.E+06	25C			0			ExtEnd	4.982E+12
LFXP2-40E	Lot #1	30	8.E+06	25C				0		ExtEnd	1.246E+13
LFXP2-40E	Lot #1	30	8.E+06	25C					0	ExtEnd	2.491E+13

CS100F Cumulative Unit Level Endurance Failure Rate = 0 / 913
CS100F Cumulative Cell Level Endurance Cycles = 9.876E+13

INDEX Return

3.4 LatticeXP2 Product Family – ESD and Latch UP Data

Electrostatic Discharge-Human Body Model:

LFXP2 product family units were tested per the Jedec JESD22-A114E Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure and Lattice Procedure # 70-100844. All units were tested at 25^0C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

LAXP2 (Automotive) product family units were tested per the JESD22-A114E and AEC-Q100-002 Human Body Model (HBM) Electrostatic Discharge (ESD) Test procedure. All units were tested at 25^0C and $+105^0$C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.1 LatticeXP2 ESD-HBM Data

Die Size	132-csBGA	144-TQFP	208-PQFP	256-ftBGA	484-ftBGA	672-ftBGA	Comments
LFXP2-5/ LAXP2-5	>1500V Jedec: Class 1C AEC-Q100-002: H1C	>1500V Jedec: Class 1C AEC-Q100-002: H1C	>1500V Jedec: Class 1C AEC-Q100-002: H1C	>2000V Jedec: Class 2 AEC-Q100-002: H2			Commercial and Automotive qualification
LFXP2-8/ LAXP2-8	>1500V Jedec: Class 1C AEC-Q100-002: H1C	>1500V Jedec: Class 1C AEC-Q100-002: H1C	>1500V Jedec: Class 1C AEC-Q100-002: H1C	>2000V Jedec: Class 2 AEC-Q100-002: H2			Commercial and Automotive qualification
LFXP2-17/ LAXP2-17			>1500V Jedec: Class 1C AEC-Q100-002: H1C	>2000V Jedec: Class 2 AEC-Q100-002: H2	>2000V Jedec: Class 2		Commercial and Automotive qualification
LFXP2-30				>1000V Jedec: Class 1C	>1000V Jedec: Class 1C	>1000V Jedec: Class 1C	Commercial qualification only
LFXP2-40				>1000V Jedec: Class 1C	>1000V Jedec: Class 1C	>1000V Jedec: Class 1C	Commercial qualification only

HBM classification for Commercial/Industrial products, per JESD22-A114E
HBM classification for Automotive products, per AEC-Q100-002

INDEX Return

Electrostatic Discharge-Machine Model:

LFXP2 product family was tested per the JESD22-A115C Electrostatic Discharge (ESD) Sensitivity Testing, Machine Model (MM) procedure.

All units were tested at 25°C and +105°C prior to reliability stress and after reliability stress. No failures were observed within the passing stress level.

Table 3.4.2 LFXP2 ESD-MM Data

Die Size	132-csBGA	144-TQFP	208-PQFP	256-ftBGA	484-ftBGA*	672-ftBGA
LFXP2-17					>50V	
LFXP2-17					>100V	
LFXP2-17					>200V	

ESD-MM stress level for Commercial/Industrial products, per JESD22-A115C
*ESD-MM stress level was performed at 3 voltages to ensure full coverage

INDEX Return

Electrostatic Discharge-Charged Device Model:

LFXP2 product family units were tested per the Jedec JESD22-C101D, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure and Lattice Procedure # 70-100844. All units were tested at 25^{0}C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

LAXP2 (Automotive) product family units were tested per the JESD22-C101D and AEC-Q100-011, Charged-Device Model (CDM) Electrostatic-Discharge (ESD) Test procedures. All units were tested at 25^{0}C and +105^{0}C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.3 LatticeXP2 ESD-CDM Data

Die Size	132-csBGA	144- TQFP	208- PQFP	256-ftBGA	484-ftBGA	672-ftBGA	Comments
LFXP2-5/ LAXP2-5	>1000V Jedec: Class IV AEC-Q100-011: C5	>1000V Jedec: Class IV AEC-Q100-011: C5	>500V Jedec: Class III AEC-Q100-011: C3A	>1000V Jedec: Class IV AEC-Q100-011: C5			Commercial and Automotive qualification
LFXP2-8/ LAXP2-8	>1000V Jedec: Class IV AEC-Q100-011: C5	>1000V Jedec: Class IV AEC-Q100-011: C5	>500V Jedec: Class III AEC-Q100-011: C3A	>1000V Jedec: Class IV AEC-Q100-011: C5			Commercial and Automotive qualification
LFXP2-17/ LAXP2-17			>750V Jedec: Class III AEC-Q100-011: C4	>500V Jedec: Class III AEC-Q100-011: C3A	>1000V Jedec: Class IV		Commercial and Automotive qualification
LFXP2-30				>500V Jedec: Class III	>500V Jedec: Class III	>500V Jedec: Class III	Commercial qualification only
LFXP2-40				>500V Jedec: Class III	>500V Jedec: Class III	>500V Jedec: Class III	Commercial qualification only

CDM classification for Commercial/Industrial products, per JESD22-C101D
CDM classification for Automotive products, per AEC-Q100-011

INDEX Return

Latch-Up:

LatticeXP2 product family units were tested per the JEDEC EIA/JESD78A IC Latch-up Test procedure and Lattice Procedure # 70-101570. All units were tested at 25^0C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

LAXP2 (Automotive) product family units were tested per the JEDEC EIA/JESD78A and AEC-Q100-004 IC Latch-up Test procedures. All units were tested at 25^0C and $+105^0$C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.4 LatticeXP2 I/O Latch Up Data

Die Size	132-csBGA	144-TQFP	208-PQFP	256-ftBGA	484-ftBGA	672-ftBGA	Comments
LFXP2-5/ LAXP2-5	> +/-100mA Jedec & AEC: Class II Level A	> +/-100mA Jedec & AEC: Class II Level A	> +/-100mA Jedec & AEC: Class II Level A	> +/-100mA Jedec & AEC: Class II Level A			Commercial and Automotive qualification
LFXP2-8/ LAXP2-8	> +/-100mA Jedec & AEC: Class II Level A	> +/-100mA Jedec & AEC: Class II Level A	> +/-100mA Jedec & AEC: Class II Level A	> +/-100mA Jedec & AEC: Class II Level A			Commercial and Automotive qualification
LFXP2-17/ LAXP2-17			> +/-100mA Jedec & AEC: Class II Level A	> +/-100mA Jedec & AEC: Class II Level A	> +/-100mA Jedec: Class II Level A		Commercial and Automotive qualification
LFXP2-30				Qualification by extension	> +/-400mA Using the old Lattice standard at room temp	> +/-400mA Using the old Lattice standard at room temp	Commercial qualification only
LFXP2-40					Qualification by extension	> +/-400mA Using the old Lattice standard at room temp	Commercial qualification only

CDM classification for Commercial/Industrial products, per JESD78A
CDM classification for Automotive products, per AEC-Q100-004

INDEX Return

Table 3.4.5 LatticeXP2 Vcc Latch Up Data

Die Size	132-csBGA	144-TQFP	208-PQFP	256-ftBGA	484-ftBGA	672-ftBGA	Comments
LFXP2-5/ LAXP2-5	> 1.5*Vcc Jedec & AEC: Class II Level A	Qualification by extension	Qualification by extension	Qualification by extension			Commercial and Automotive qualification
LFXP2-8/ LAXP2-8	> 1.5*Vcc Jedec & AEC: Class II Level A	Qualification by extension	Qualification by extension	Qualification by extension			Commercial and Automotive qualification
LFXP2-17/ LAXP2-17			Qualification by extension	> 1.5*Vcc Jedec & AEC: Class II Level A	> 1.5*Vcc Jedec: Class II Level A		Commercial and Automotive qualification
LFXP2-30				Qualification by extension	Qualification by extension	> 1.5*Vcc Jedec: Class II Level A	Commercial qualification only
LFXP2-40					Qualification by extension	> 1.5*Vcc Jedec: Class II Level A	Commercial qualification only

Latch Up Classification: The two main classes are Class I for latch-up at room-temperature and Class II for Latch-Up at the maximum-rated ambient temperature. Within Class I and Class II are two trigger current levels. For the I-test the Level A trigger current is +/-100mA. Level B is for the purpose of defining and reporting a higher or lower injection current value as appropriate. Earlier latch-up testing at Lattice was hardware limited to room temperature testing only. Additionally, maximum-rated ambient temperature latch-up testing is generally considered to be approximately 2X worse than the trigger values found at room temperature. In order to guard band our room temperature latch-up testing the standard was 4X, or +/- 400mA trigger current. Therefore, the previous Lattice I/O LU standard was >400mA at room temperature, while the present standard is >100mA at maximum-rated ambient temperature.

INDEX Return

4.0 PACKAGE QUALIFICATION DATA FOR LatticeXP2 PRODUCT FAMILY

The LFXP2 and LAXP2 (Automotive) product families are offered in ftBGA, csBGA, fpBGA PQFP and TQFP packages. To cover the range of die in the largest package types for this product family, different package and die combinations were chosen as the generic qualification vehicles for all the package qualification tests including, Temperature Cycling (T/C), Un-biased HAST (UHAST)and Biased HAST (BHAST). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection.

The generation and use of generic data is applied across a family of products or packages emanating from one base wafer foundry or assembly process is a Family Qualification, or Qualification By Extension. For the package stresses BHAST and UHAST, these are considered generic for a given Package Technology. T/C is considered generic up to an evaluated die size + package size + 10%, for a given Package Technology. Surface Mount Pre-Conditioning (SMPC) is considered generic up to an evaluated Peak Reflow temperature, for a given Package Technology. The following table demonstrates the package qualification matrix.

Table 4.1 Product-Package Qualification-By-Extension Matrix

<table>
<tr><td colspan="2"></td><td colspan="2">ASEM /UTAC</td><td colspan="4">ASEM/UTAC</td></tr>
<tr><td>Product</td><td>Stress Test</td><td>144-TQFP</td><td>208-PQFP</td><td>132-csBGA</td><td>256-ftBGA</td><td>484-fpBGA</td><td>672-fpBGA</td></tr>
<tr><td rowspan="5">LFXP2-40</td><td>SMPC</td><td colspan="4" rowspan="5">Package not offered</td><td rowspan="11">Qualified by extension</td><td>MSL3</td></tr>
<tr><td>T/C</td><td>1K CYC</td></tr>
<tr><td>BHAST</td><td>By Extension</td></tr>
<tr><td>UHAT</td><td>By Extension</td></tr>
<tr><td>*HTSL</td><td>1K HRS</td></tr>
<tr><td rowspan="5">LFXP2-30</td><td>SMPC</td><td colspan="3" rowspan="5">Package not offered</td><td>MSL3</td><td rowspan="5">Qualified by extension</td></tr>
<tr><td>T/C</td><td>1K CYC</td></tr>
<tr><td>BHAST</td><td>By Extension</td></tr>
<tr><td>UHAST</td><td>By Extension</td></tr>
<tr><td>*HTSL</td><td>By Extension</td></tr>
<tr><td rowspan="5">LFXP2-17/
LAXP2-17</td><td>SMPC</td><td rowspan="5">Package not offered</td><td>MSL3</td><td rowspan="5">Qualified by extension</td><td>MSL3</td><td rowspan="5">Package not offered</td></tr>
<tr><td>T/C</td><td>1K CYC</td><td>1K CYC</td></tr>
<tr><td>BHAST</td><td>96 HRS</td><td>96 HRS</td></tr>
<tr><td>UHAST</td><td>96 HRS</td><td>96 HRS</td></tr>
<tr><td>*HTSL</td><td>By Extension</td><td>1K HRS</td></tr>
<tr><td rowspan="5">LFXP2-8/
LAXP2-8</td><td>SMPC</td><td>MSL3</td><td rowspan="5">Qualified by extension</td><td>MSL3</td><td rowspan="5">Qualified by extension</td><td colspan="2" rowspan="5">Package not offered</td></tr>
<tr><td>T/C</td><td>1K CYC</td><td>1K CYC</td></tr>
<tr><td>BHAST</td><td>96 HRS</td><td>96 HRS</td></tr>
<tr><td>UHAST</td><td>96 HRS</td><td>96 HRS</td></tr>
<tr><td>*HTSL</td><td>By Extension</td><td>By Extension</td></tr>
<tr><td rowspan="5">LFXP2-5/
LAXP2-5</td><td>SMPC</td><td>MSL3</td><td>MSL3</td><td rowspan="5">Qualified by extension</td><td colspan="2" rowspan="5">Package not offered</td></tr>
<tr><td>T/C</td><td>1K CYC</td><td>1K CYC</td></tr>
<tr><td>BHAST</td><td>96 HRS</td><td>96 HRS</td></tr>
<tr><td>UHAST</td><td>96 HRS</td><td>96 HRS</td></tr>
<tr><td>*HTSL</td><td>1K HRS</td><td>1K HRS</td></tr>
</table>

Note – Qualified by extension is from the largest die/package combination
* For the non-volatile based products, the HTRX and HTSL stress and test conditions condition are the same. Therefore in some cases, the HTSL test is covered by the HTRX stress.

INDEX Return

4.1 LatticeXP2 Product Family Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JEDEC JESD22-A113 “Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing”, Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

Surface Mount Preconditioning (MSL3)
(10 Temperature Cycles, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, 245/250/260 °C Reflow Simulation, 3 passes) performed before all CS100F package tests.
MSL3 Packages: TQFP, PQFP, fpBGA, ftBGA, csBGA
Method: Lattice Procedure # 70-103467, J-STD-020 and JESD22-A113

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LAXP2-17E	256 ftbGA	ASEM	Lot #8	231	0	260°C
LAXP2-17E	256 ftbGA	ASEM	Lot #9	316	0	260°C
LAXP2-17E	256 ftbGA	ASEM	Lot #10	304	0	260°C
LFXP2-30E	256 ftbGA	ASEM	Lot #1	84	0	260°C
LFXP2-30E	256 ftbGA	ASEM	Lot #2	84	0	260°C
LAXP2-5E	144 TQFP	ASEM	Lot #1	235	0	260°C
LAXP2-5E	144 TQFP	ASEM	Lot #2	315	0	260°C
LFXP2-5E	144 TQFP	ASEM	Lot #3	75	0	260°C
LFXP2-40E	672 fpBGA	ASEM	Lot #1	78	0	250°C
LFXP2-40E	672 fpBGA	ASEM	Lot #2	80	0	250°C
LFXP2-8E	132 csBGA	ASEM	Lot #1	154	0	260°C
LFXP2-8E	132 csBGA	ASEM	Lot #2	154	0	260°C
LFXP2-8E	132 csBGA	ASEM	Lot #3	247	0	260°C
LAXP2-8E	144 TQFP	ASEM	Lot #5	231	0	260°C
LAXP2-8E	144 TQFP	ASEM	Lot #6	126	0	260°C
LAXP2-8E	144 TQFP	ASEM	Lot #7	80	0	260°C
LFXP2-17E	208 PQFP	ASEM	Lot #1	48	0	245°C
LFXP2-17E	208 PQFP	ASEM	Lot #2	47	0	245°C
LFXP2-17E	208 PQFP	ASEM	Lot #3	47	0	245°C
LAXP2-17E	208 PQFP	ASEM	Lot #11	79	0	260°C
LAXP2-17E	208 PQFP	ASEM	Lot #12	80	0	260°C
LAXP2-17E	208 PQFP	ASEM	Lot #13	77	0	260°C
LAXP2-5E	208 PQFP	ASEM	Lot #1	238	0	260°C
LAXP2-5E	208 PQFP	ASEM	Lot #2	239	0	260°C
LAXP2-5E	208 PQFP	ASEM	Lot #4	234	0	260°C
LFXP2-5E	144 TQFP	UTAC	Lot #1	77	0	260°C
LFXP2-5E	144 TQFP	UTAC	Lot #2	77	0	260°C
LFXP2-5E	144 TQFP	UTAC	Lot #3	77	0	260°C
LFE2-12E	144 TQFP	UTAC	Lot #4	77	0	260°C

INDEX Return

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LFE2-12E	144 TQFP	UTAC	Lot #5	77	0	260°C
LFE2-12E	144 TQFP	UTAC	Lot #6	77	0	260°C
LFXP2-8E	256 ftBGA	UTAC	Lot #1	77	0	260°C
LFXP2-8E	256 ftBGA	UTAC	Lot #2	77	0	260°C
LFXP2-8E	256 ftBGA	UTAC	Lot #3	77	0	260°C
LFXP2-8E	132 csBGA	UTAC	Lot #1	77	0	260°C
LFXP2-8E	132 csBGA	UTAC	Lot #2	77	0	260°C
LFXP2-8E	132 csBGA	UTAC	Lot #3	77	0	260°C
LFE2M35SE	256 ftBGA	UTAC	Lot #1	77	0	260°C
LFE2M35SE	256 ftBGA	UTAC	Lot #2	77	0	260°C

Cumulative SMPC Failure Rate = 0 / 4,961

INDEX Return

4.2 LatticeXP2 Product Family Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104 "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, PQFP, fpBGA, ftBGA, csBGA
Stress Duration: 1000 cycles
Stress Conditions: Temperature cycling between -55°C to 125°C (Condition B)
Method: Lattice Procedure # 70-101568 and JESD22-A104

Table 4.2.1: Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Quantity	250 Cycles	500 Cycles	1000 Cycles
LAXP2-17E	256 ftbGA	ASEM	Lot #8	77	0	0	0
LAXP2-17E	256 ftbGA	ASEM	Lot #9	156	0	0	0
LAXP2-17E	256 ftbGA	ASEM	Lot #10	74	0	0	0
LFXP2-30E	256 ftbGA	ASEM	Lot #1	84	0	0	0
LFXP2-30E	256 ftbGA	ASEM	Lot #2	84	0	0	0
LAXP2-5E	144 TQFP	ASEM	Lot #2	75	0	0	0
LAXP2-5E	144 TQFP	ASEM	Lot #4	80	0	0	0
LFXP2-40E	672 fpBGA	ASEM	Lot #1	78	0	0	0
LFXP2-40E	672 fpBGA	ASEM	Lot #2	80	0	0	0
LFXP2-8E	132 csBGA	ASEM	Lot #1	77	0	0	0
LFXP2-8E	132 csBGA	ASEM	Lot #2	77	0	0	0
LFXP2-8E	132 csBGA	ASEM	Lot #3	77	0	0	0
LAXP2-8E	144 TQFP	ASEM	Lot #5	78	0	0	0
LAXP2-8E	144 TQFP	ASEM	Lot #6	80	0	0	0
LAXP2-8E	144 TQFP	ASEM	Lot #7	80	0	0	0
LAXP2-17E	208 PQFP	ASEM	Lot #11	79	0	0	0
LAXP2-17E	208 PQFP	ASEM	Lot #12	80	0	0	0
LAXP2-17E	208 PQFP	ASEM	Lot #13	77	0	0	0
LAXP2-5E	208 PQFP	ASEM	Lot #1	79	0	0	0
LAXP2-5E	208 PQFP	ASEM	Lot #2	80	0	0	0
LAXP2-5E	208 PQFP	ASEM	Lot #4	77	0	0	0
LFE2-12E	144 TQFP	UTAC	Lot #4	77	0	0	0
LFE2-12E	144 TQFP	UTAC	Lot #5	77	0	0	0
LFE2-12E	144 TQFP	UTAC	Lot #6	77	0	0	0
LFE2M35SE	256 ftBGA	UTAC	Lot #1	77	0	0	0
LFE2M35SE	256 ftBGA	UTAC	Lot #2	77	0	0	0

Cumulative Temp Cycle Failure Rate = 0 / 2,114

INDEX Return

4.3 LatticeXP2 Product Family Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent JEDEC JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," the Unbiased HAST conditions are 96 hour exposure at 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, PQFP, fpBGA, ftBGA, csBGA
Stress Duration: 96 Hrs
Stress Conditions: 130°C, 15psig, 85% RH
Method: Lattice Procedure # 70-104285 and JESD22-A118

Table 4.3.1: Unbiased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LAXP2-17E	256 ftbGA	ASEM	Lot #8	77	0	96 Hrs
LAXP2-17E	256 ftbGA	ASEM	Lot #9	80	0	96 Hrs
LAXP2-17E	256 ftbGA	ASEM	Lot #10	77	0	96 Hrs
LAXP2-5E	144 TQFP	ASEM	Lot #2	80	0	96 Hrs
LAXP2-5E	144 TQFP	ASEM	Lot #4	80	0	96 Hrs
LFXP2-8E	132 csBGA	ASEM	Lot #1	77	0	96 Hrs
LAXP2-8E	144 TQFP	ASEM	Lot #5	76	0	96 Hrs
LAXP2-5E	208 PQFP	ASEM	Lot #1	79	0	96 Hrs
LAXP2-5E	208 PQFP	ASEM	Lot #2	79	0	96 Hrs
LAXP2-5E	208 PQFP	ASEM	Lot #4	78	0	96 Hrs
LFXP2-8E	132 csBGA	UTAC	Lot #1	77	0	96 Hrs
LFXP2-8E	132 csBGA	UTAC	Lot #2	77	0	96 Hrs
LFXP2-8E	132 csBGA	UTAC	Lot #3	77	0	96 Hrs

Cumulative Unbiased HAST failure Rate = 0 / 1,014

INDEX Return

4.4 LatticeXP2 Product Family THB: Biased HAST Data

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD A110-B "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are with Vcc bias and alternate pin biasing in an ambient of 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, PQFP, fpBGA, ftBGA, csBGA
Stress Conditions: Vcc= 1.26V/ V_{CCIO} = 3.47V, 130°C / 85% RH, 15 psig
Stress Duration: 96 hours
Method: Lattice Procedure # 70-101571 and JESD22-A101B

Table 4.4.1: Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LAXP2-17E	256 ftbGA	ASEM	Lot #8	77	0	96 Hrs
LAXP2-17E	256 ftbGA	ASEM	Lot #9	80	0	96 Hrs
LAXP2-17E	256 ftbGA	ASEM	Lot #10	77	0	96 Hrs
LAXP2-5E	144 TQFP	ASEM	Lot #2	80	0	96 Hrs
LAXP2-5E	144 TQFP	ASEM	Lot #4	80	0	96 Hrs
LFXP2-8E	132 csBGA	ASEM	Lot #2	77	0	96 Hrs
LFXP2-8E	132 csBGA	ASEM	Lot #3	170	1[A]	96 Hrs
LAXP2-8E	144 TQFP	ASEM	Lot #5	77	0	96 Hrs
LAXP2-5E	208 PQFP	ASEM	Lot #1	80	0	96 Hrs
LAXP2-5E	208 PQFP	ASEM	Lot #2	80	0	96 Hrs
LAXP2-5E	208 PQFP	ASEM	Lot #4	79	0	96 Hrs
LFXP2-5E	144 TQFP	UTAC	Lot #1	77	0	96 Hrs
LFXP2-5E	144 TQFP	UTAC	Lot #2	77	0	96 Hrs
LFXP2-5E	144 TQFP	UTAC	Lot #3	77	0	96 Hrs
LFXP2-8E	256 ftBGA	UTAC	Lot #1	77	0	96 Hrs
LFXP2-8E	256 ftBGA	UTAC	Lot #2	77	0	96 Hrs
LFXP2-8E	256 ftBGA	UTAC	Lot #3	77	0	96 Hrs

A – 1 unit failed BHAST for pair of Open pins due to EOS. FAR#: 1375

Cumulative BHAST failure Rate = 1 / 1,419

INDEX Return

5.0 CS100F Process Reliability Wafer Level Review

Several key fabrication process related parameters have been identified by the foundry that would affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. Normal operating conditions are defined in the Electrical Design Rules (EDR). These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence.

Table 5.1 – Wafer Level Reliability Results

HCI

Device	LVN	LVP	MVN	MVP	HVN	HVP
delta Ids	-10%	-10%	-10%	-10%	-10%	-10%
Celsius	25	25	25	25	25	25
Vgstress	Vd/2	Vd	Vd/2	Vd	Vd/2	Vd
Vds	1.26	-1.26	3.465	-3.465	5.25	-5.25
TTF	3 lots>15yr	3 lots>27,000yr	3 lots>79yr	3 lots>14Myr	3 lots>67yr	3 lots>11,000yr

TDDB

Device	LVN	LVP	MVN	MVP	HVN	HVP	Intermed. IMD
Celsius	125	125	125	125	125	125	125
Vg	1.26	-1.26	3.465	-3.465	5.25	-5.25	3.465
Max Area	0.11cm^2	0.13cm^2	0.005cm^2	0.0071cm^2	9.5e-5cm^2	4.34e-5cm^2	L/S=140nm
0.1% TTF	3 lots>3300yr	3 lots>7200yr	3 lots>40yr	3 lots>86yr	3 lots>177yr	3 lots>18yr	6 lots>40yr

NBTI

Device	LVP	MVP	HVP
delta Vth	50mv	100mv	100mv
Celsius	125	125	125
Vg	-1.26	-3.465	-5.25
TTF	3 lots>39yr	3 lots>6Myr	3 lots>130yr

EML

Device	Intermediate	Semi-Global	Global	Top Al
Celsius	125	125	125	125
delta R	+5%	+5%	+5%	+5%
Jmax	3e5A/cm^2	3e5A/cm^2	3e5A/cm^2	2.5e5A/cm^2
0.1% TTF	6 lots>14yr	6 lots>16yr	6 lots>24yr	4 lots>14yr

SM

Device	Intermediate	Semi-Global	Global
delta R	+100%	+100%	+100%
Celsius	125	125	125
TTF	6 lots>118yr	6 lots>36yr	6 lots>48yr

Note: Reliability life times are based on listed temperature and use conditions. Detailed WLR test conditions and report are available upon request.

INDEX Return

6.0 LatticeXP2 Soft Error Data

Soft Error Rate testing is conducted to characterize the sensitivity of SRAM storage and device logic elements to High Energy Neutron and Alpha Particle radiation. Charge induced by the impact of these particles can collect at sensitive nodes in the device, and result in changes in the internal electrical states of the device. While these changes do not cause physical damage to the device, they can cause a logical error in device operation.

All testing conforms to JEDEC JESD-89.

Table 6.1 XP2 MEASURED FITs / Mb

Stress / Structure	FLASH	CONFIGURATION	EBR
Neutron	0	99	168
Alpha	0	173	273

Note: Detailed SER data report is available upon request.

INDEX Return

7.0 LatticeXP2 PACKAGE ASSEMBLY INTEGRITY TESTS

7.1 Wire Bond Shear Test

This procedure is used to measure the wire bond strength at the ball joints. Thirty bonds from a minimum of five devices were used for Wire Bond Shear.

WIRE BOND SHEAR TEST RESULTS: All bond shear observations were > 18 grams for TQFP, PQFP, csBGA and ftBGA packages tested.

The average measured bond shear results for 144 pin TQFP were Cpk of > 7.7 and Ppk of > 4.4.
The average measured bond shear results for 208 pin PQFP were Cpk of > 5.9 and Ppk of > 4.2.
The average measured bond shear results for 132 ball csBGA were Cpk of > 8.9 and Ppk of > 6.8.
The average measured bond shear results for 256 ball ftBGA were Cpk of > 9.5 and Ppk of > 4.5

7.2 Wire Bond Pull

This procedure is used to measure the wire bond strength at the ball joints and stitch bonds.
For products evaluation thirty bonds from a minimum of five devices were used for and Wire Bond Pull. Test conditions for these tests were 6 grams minimum for 1.0 mil gold wire

WIRE BOND PULL RESULTS: All bond pull observations were >6 grams for TQFP and ftBGA packages tested.

The average measured wire bond pull results for 144 pin TQFP were Cpk of > 5.3 and Ppk of > 2.6.
The average measured wire bond pull results for 208 pin PQFP were Cpk of > 4.3 and Ppk of > 2.5.
The average measured wire bond pull results for 132 ball csBGA were Cpk of > 5.3 and Ppk of > 2.6.
The average measured wire bond pull results for 256 ball ftBGA were Cpk of > 2.4 and Ppk of > 1.8.

7.3 Solderability

This procedure is used to evaluate the solderability of device terminals normally joined by a soldering operation. An accelerated aging test is included in this test method, which simulates natural aging under a combination of various storage conditions that have deleterious effects. Units are exposed to a 8 hour steam preconditioning followed a flux exposure for 7 seconds and a dip in Pb-free solder alloy @ 245 °C ± 5°C for 5 seconds. Minimum of 22 leads from 3 devices per lot were tested with zero failure acceptance.

No failures were observed for LatticeXP2 devices in TQFP and PQFP packages. All the tested units passed. There was less than 5% pitting and dewetting on the solder covered area.

7.4 Physical Dimensions

Devices were measured using the appropriate Lattice Semiconductor case outline drawings.

The 10 devices from 3 different lots for each package type were measured with no failures found.
The 144 pin TQFP calculated Cpk is > 3.5 and Ppk > 3.4.
The 208 pin PQFP calculated Cpk is > 3.0 and Ppk > 1.7.
The 132 ball csBGA calculated Cpk is > 6.1 and Ppk > 2.4.
The 256 ball ftBGA calculated Cpk is > 100 and Ppk > 100.

INDEX Return

7.5 Solder Ball Shear

For the 132 ball csBGA and 256 ball ftBGA packages, ten devices from three lots were tested. All units were exposed to two surface mount reflow simulations.

The 132 ball csBGA packages use a 0.40 mm barrier metal diameter. All ball shear observations were > 315 grams.

The 256 ball ftBGA packages use a 0.40 mm barrier metal diameter. All ball shear observations were > 725 grams.

The average measured ball shear results for 132 ball csBGA packages post reflow stress were Cpk of > 1.9 and Ppk of > 1.4.

The average measured ball shear results for 256 ball ftBGA packages post reflow stress were Cpk of > 5.5 and Ppk of > 4.1.

INDEX Return

8.0 LatticeXP2 ADDITIONAL FAMILY DATA

Table 8.1: LFXP2 and LA-XP2 (Automotive) Package Assembly Data – csBGA/ ftBGA/ fpBGA

Package Attributes / Assembly Sites	ASEM	UTAC
Die Family (Product Line)	LatticeXP2	LatticeXP2
Fabrication Process Technology	CS100F (90nm CMOS)	CS100F 90nm CMOS)
Package Assemble Site	Malaysia	Singapore
Package Type	csBGA/ftBGA/fpBGA	csBGA/ftBGA
Ball Counts	132/256/484/672	132/256
Die Preparation/Singulation	wafer saw, full cut	wafer saw, full cut
Die Attach Material	Ablebond 2100 Series	Ablebond 2100 Series
Mold Compound Supplier/ID	Hitachi 9750HF Series	Hitachi 9750HF Series
Wire Bond Material	Gold (Au)	Gold (Au)
Wire Bond Methods	Thermosonic Ball	Thermosonic Ball
Substrate Material	Bismaleimide Triazine HL83X Series	Bismaleimide Triazine HL83X Series
L/F Plating or BGA Ball	Sn96.5/Ag3.0/Cu0.5	Sn96.5/Ag3.0/Cu0.5
Lead Finish	SnAgCu solder ball	SnAgCu solder ball
Marking	Laser	Laser

Table 8.2: LFXP2 and LA-XP2 (Automotive) Package Assembly Data- TQFP

Package Attributes / Assembly Sites	ASEM	UTAC
Die Family (Product Line)	LatticeXP2	LatticeXP2
Fabrication Process Technology	CS100F (90nm CMOS)	CS100F (90nm CMOS)
Package Assembly Site	Malaysia	Singapore
Package Type	TQFP/PQFP	TQFP
Pin Count	144/208	144
Die Preparation/Singulation	wafer saw, full cut	wafer saw, full cut
Die Attach Material	Ablebond 3230	Ablebond 3230
Mold Compound Supplier/ID	Hitachi 9510HF Series	Hitachi 9510HF Series
Wire Bond Material	Gold (Au)	Gold (Au)
Wire Bond Methods	Thermosonic Ball	Thermosonic Ball
Lead frame Material	Cu Alloy	Cu Alloy
Lead Finish	Matte Sn (annealed)	Matte Sn (annealed)
Marking	Laser	Laser

INDEX Return

9.0 Revision History

Table 9.1: LatticeXP2 Product Family Qualification Summary Revisions

Date	Revision	Request	Section	Change Summary
February 2008	A	9906		New Release
March 2008	B	9925		Updated test methods and qual data
May 2008	C	9990		Added XP2-30E, FTN256 temp cycle extension data
July 2009	D	10318		Update qual summary data and format
November 2012	E	DMS-474	2.2, 3.4	Update Table 2.2 to add ESD-MM information. Update 3.4 to add Electrostatic Discharge-Machine Model data and table. Administrative change to add document wrapper.

INDEX Return

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