Lattice Die Sale Data Sheet (Including Known Good Die)

DS1051 Version 1.0, March 2015

Lattice Die Sale Data Sheet

March 2015 **Data Sheet DS1051**

Die Product Offering

Lattice offers its most popular CPLDs and FPGAs in Die form. These Die products offer a wide range of logic densities, I/Os, high performance SERDES channels, memory resources, PLLs and multipliers. Some product are non-volatile, infinitely programmable and others are volatile in nature.

Table 1 below highlights the specific products offered by Lattice in Die form, including their associated ordering part numbers (OPNs). The table provides a high level summary of some of the product family features. For a comprehensive understanding of each family's capabilities, please refer to the individual device family data sheets on the Lattice web site.

Table 1. Lattice Die Offering

Family	Density (LUTs)	Speed Grade	Test Method	I/Os + Ded. I/Os	Serdes	Dist'd RAM (Kbits)	EBR SRAM (Kbits)	PLLs/ DLLs	18x18 Mult's	Ordering Part Number (OPN)	Lithography (nm)	Programmability	Wafer Dia. (mm)
MachXO2™ HC MachXO2 HE MachXO2 ZE	256	–4 –1	Known Good Die	55	None	2	0	0	None	LCMXO2-256HC DIE LCMXO2-256ZE DIE	65	Non-Volatile Infinitely Reconfig	300
	640	–4 –1		79		5	18	0		LCMXO2-640HC DIE LCMXO2-640ZE DIE			
	1280	–4 –1		107		10	64	1		LCMXO2-1200HC DIE LCMXO2-1200ZE DIE			
	2112	–4 –4 –1		206		16	74	1		LCMXO2-2000HC DIE LCMXO2-2000HE DIE LCMXO2-2000ZE DIE			
	4320	–4 –4 –1		278		34	92	2		LCMXO2-4000HC DIE LCMXO2-4000HE DIE LCMXO2-4000ZE DIE			
	6864	–4 –4 –1		334		54	240	2		LCMXO2-7000HC DIE LCMXO2-7000HE DIE LCMXO2-7000ZE DIE			
MachXO™	256	–3	Lattice Good Die	78	None	2	0	0	None	LCMXO256C DIE LCMXO256E DIE	130	Non-Volatile Infinitely Reconfig	300
	640			159		6.1	0	0		LCMXO640C DIE LCMXO640E DIE			
	1200			211		6.4	9.2	1		LCMXO1200C DIE LCMXO1200E DIE			
	2280			271		7.7	27.6	2		LCMXO2280C DIE LCMXO2280E DIE			

Family	Density (LUTs)	Speed Grade	Test Method	I/Os + Ded. I/Os	Serdes	Dist'd RAM (Kbits)	EBR SRAM (Kbits)	PLLs/ DLLs	18x18 Mult's	Ordering Part Number (OPN)	Lithog-raphy (nm)	Program-mability	Wafer Dia. (mm)
LatticeXP2™	5K	–5	Lattice Good Die	172	None	10	166	2	None	LFXP2-5E DIE	90	Non-Volatile Infinitely Reconfig	300
	8K			201		18	221	2		LFXP2-8E DIE			
	17K			358		35	276	4		LFXP2-17E DIE			
	29K			472		56	387	4		LFXP2-30E DIE			
	40K			540		83	885	4		LFXP2-40E DIE			
ECP5™ (LEF5U)	24K	–6	Known Good Die	197	None	194	1008	2/2	28	FE5U-25F DIE	40	Volatile	300
	44K			245		351	1944	4/4	72	FE5U-45F DIE			
	84K			365		669	3744	4/4	156	FE5U-85F DIE			
ECP5 (LFE5UM)	24K	–6	Known Good Die	197	2	194	1008	2/2	28	FE5UM-25F DIE	40	Volatile	300
	44K			245	4	351	1944	4/4	72	FE5UM-45F DIE			
	84K			365	4	669	3744	4/4	156	FE5UM-85F DIE			
LatticeECP3™	17K	–6	Known Good Die	222	4	36	700	2/2	24	LFE3-17EA DIE	65	Volatile	300
	33K			310	4	68	1327	4/2	64	LFE3-35EA DIE			
	67K			490	12	145	4420	10/2	128	LFE3-70EA DIE			
	92K			490	12	188	4420	10/2	128	LFE3-95EA DIE			
	149K			586	16	303	6850	10/2	320	LFE3-150EA DIE			
LatticeECP2™	6K	–5	Lattice Good Die	190	None	12	55	2/2	12	LFE2-6SE DIE	90	Volatile	300
	12K			297		24	221	2/2	24	LFE2-12SE DIE			
	21K			402		42	276	2/2	28	LFE2-20SE DIE			
	32K			450		64	332	2/2	32	LFE2-35SE DIE			
	48K			500		96	387	4/2	72	LFE2-50SE DIE			
	68K			583		136	1032	6/2	88	LFE2-70SE DIE			
LatticeECP2M™	19K	–5	Lattice Good Die	304	4	41	1217	8/2	24	LFE2M-20SE DIE	90	Volatile	300
	34K			410	4	71	2101	8/2	32	LFE2M-35SE DIE			
	48K			410	8	101	4147	8/2	88	LFE2M-50SE DIE			
	67K			436	16	145	4534	8/2	96	LFE2M-70SE DIE			
	95K			520	16	202	5308	8/2	168	LFE2M-100SE DIE			
ispMACH® 4000ZE	32	–4	Lattice Good Die	32+4	None	None	None	None	None	LC4032ZE DIE	180	Non-Volatile Infinitely Reconfig	200
	64			64+10						LC4064ZE DIE			
	128	–5		96+4						LC4128ZE DIE			
	256			108+4						LC4256ZE DIE			

Product Test Methodology

Lattice supports two wafer test methodologies. Our newer product families utilize a *Known Good Die (KGD)* test methodology where most of the testing that used to be performed post-assembly during packaged final test has been pulled into our wafer-level test process. The KGD wafer level testing is performed at both hot and cold with two separate test insertions (Sort 1 and Sort 2). For non-volatile process technologies, there is a third test insertion (Sort 3), performed at room temperature to complete the data retention testing.

The KGD wafer level test covers both AC and DC performance specifications as well as the performance of key functional blocks such as configuration memory, block memory, PLLs, multipliers and programmable interconnects.

It should be noted that even though the KGD test flow is more comprehensive than the Lattice Good Die flow (described in next section), it does not test 100% of the data sheet parameters. There are still some tests which can only be performed in a packaged configuration, during final test, when there is full access to all I/O pins.

A summary of the device parameters tested via the KGD wafer test flow are listed in Table 2 below.

Table 2. Known Good Die (KGD) Wafer Test Coverage[1]

Parameter	MachXO2			LatticeECP3		ECP5 (LFE5UM)		ECP5 (LFE5U)	
	KGD Sort 1	KGD Sort 2	KGD Sort 3	KGD Sort 1	KGD Sort 2	KGD Sort 1	KGD Sort 2	KGD Sort 1	KGD Sort 2
Test Temp	Cold	Hot	Room	Hot	Cold	Cold	Hot	Cold	Hot
Continuity	Partial[2]	Partial[2]	n/a Data Retention Only	Partial[2]	Partial[2]	Partial[2]	Partial[2]	Partial[2]	Partial[2]
Leakage	None	None		Partial	Partial	Partial	Partial	Partial	Partial
Icc	Full	Full		Full	Full	Full	Full	Full	Full
AC	Full	Full		Full	Full	Full	Full	Full	Full
Configuration Memory	Full	Full		Full	Full	Full	Full	Full	Full
Fabric/Routing	Full	Full		Full	Full	Full	Full	Full	Full
Phase Lock Loop (PLL)	Full	Full		None	None	Full	Full	Full	Full
DSP (Multipliers)	FNA	FNA		Full	Full	Full	Full	Full	Full
Programmable Interconnect (PIC)	Full[3]	Full[3]		Full	Full	Full	Full	Full	Full
Embedded Block RAM (EBR)	Full	Full		Full	Full	Full	Full	Full	Full
IO Functionality	Full	Full		Full	Full	Full	Full	Full	Full
SERDES	FNA	FNA		None	None	Partial	Partial	FNA	FNA
Flash Trim	Full	Full		FNA	FNA	FNA	FNA	FNA	FNA
Data Retention	n/a	Pgm'd State	Erased State	FNA	FNA	FNA	FNA	FNA	FNA

1. FNA – Function Not Available
   n/a – Wafer sort test is Not Applicable (test not needed or already completed)
   Full – Function fully tested during wafer sort
   None – Function available, but not tested during wafer sort
   Partial – Function available, only partially tested during wafer sort
2. Not all pins are accessible at wafer sort.
3. Fully tested as of 2Q15.

Lattice's second wafer test methodology is referred to as the *Lattice Good Die (LGD)* test methodology. It is a more traditional wafer testing process that primarily tests DC parameters to ensure basic device functionality. Once functionality has been established, Lattice is able to guarantee AC performance to the slowest commercial speed grade by virtue of our initial device characterization testing.

A summary of the device parameters tested via the LGD wafer test flow are listed in Table 3 below.

Table 3. Lattice Good Die (LGD) Wafer Test Coverage[1]

Parameter	MachXO			LatticeXP2			ispMACH4000ZE			Lattice ECP2	Lattice ECP2M
	LGD Sort 1	LGD Sort 2	LGD Sort 3	LGD Sort 1	LGD Sort 2	LGD Sort 3	LGD Sort 1	LGD Sort 2	LGD Sort 3	LGD Sort 1	LGD Sort 1
Test Temp	Room	Room	Room	Room	Room	Room	Room	Room	Room	Room	Room
Continuity	Partial[2]	n/a Data Retention Only	n/a Data Retention Only	Partial[2]	n/a Data Retention Only	n/a Data Retention Only	Partial[2]	n/a Data Retention Only	n/a Data Retention Only	Partial[2]	Partial[2]
Leakage	Partial			Partial			Partial			Partial	Partial
Icc	Full			Full			Full			Full	Full
AC	None			None			None			None	None
Configuration Memory	Full			Full			Full			Full	Full
Fabric/Routing	Full			Full			Full			Full	Full
Phase Lock Loop (PLL)	None			Partial[2]			FNA			Partial	Partial
DSP (Multipliers)	FNA			FNA			FNA			Full	Full
Programmable Interconnect (PIC)	Partial			Partial			Partial			Partial	Partial
Embedded Block RAM (EBR)	Partial			Partial			FNA			Full	Full
IO Functionality	Partial			Partial			Partial			Partial	Partial
SERDES	FNA			FNA			FNA			FNA	None
Flash Trim	Full			Full			Full			FNA	FNA
Data Retention	n/a	Pgm'd State	Erased State	n/a	Pgm'd State	Erased State	n/a	Pgm'd State	Erased State	FNA	FNA

1. FNA – Function Not Available
   n/a – Wafer sort test is Not Applicable (test not needed or already completed)
   Full – Function fully tested during wafer sort
   None – Function available, but not tested during wafer sort
   Partial – Function available, only partially tested during wafer sort
2. Not all pins accessible at wafer sort.

Speed and Temperature Grade Offering

The guaranteed speed and temperature grades are a function of the Test Methodology and are summarized in the table below:

Table 4. Speed and Temperature Grades

Test Methodology	Speed Grade	Temperature Range
KGD	Slowest	Industrial
LGD	Slowest	Commercial

Maximum Conditions

Table 5. MAX Temperature Ratings

	Wafer bumping for flip chip packaging or flip chip on board	Fan-in (WLCSP) or Fan-out (FO-WLCSP) Wafer Level Chip Scale Package	Quad Flatpack (QFP) or Quad Flatpack No-Lead (QFN)	Wirebond, Ball Grid Array Package with Laminate Substrate (LBGA)	Multi-chip Package (MCP) or System-in-Package (SiP)
MAX Temperature Rating by Package Technology	375 °C MAX for cure of polymer redistribution layers composed of PI/ polyimide 260 °C MAX for reflow of Pb-free solder bumps to customer's substrate or printed circuit board	320 °C MAX for cure of polymer redistribution layers composed of PBO/ polybenzobisoxazole Lattice does not recommend use of polyimide for redistribution layers on WLCSP packages since PBO offers improved board-level reliability 260 °C MAX for reflow of Pb-free solder balls to customer's printed circuit board	200 °C MAX at wirebond 180 °C MAX at mold cure	170 °C MAX for package substrate thickness < 0.56 mm 180 °C MAX for package substrate thickness ≥ 0.56 mm	200 °C MAX for wirebond of Lattice die (Lattice does not recommend wirebond after redistribution layers are applied) 260 °C MAX for reflow of Lattice die with: a) Pb-free solder bumps; b) Cu pillars with Pb-free solder tips; or c) WLCSP with Pb-free solder balls: For integration of Lattice die with Au stud bumps or Cu pillars without Pb-free solder tips: 400 °C MAX

- Die Programming Temperature – Commercial Temperature Range (0 °C - 70 °C)
- All Device-specific data sheet specifications regarding Absolute Maximum Ratings and Recommended Operating Conditions should be adhered to.

Reference Documents

- Pin Tables for each device are located on the Lattice web site under the Die Sale page or can be made available through your Lattice Sales Representative.
- Device dimensional data is also available on the Lattice web site under the Die Sale page or can be made available through your Lattice Sales Representative.

Definition of Terms

CM – Contract Manufacturer: This is an optional participant to the Die manufacturing process. The CM will be adding significant value to the Die by incorporating the Die into a package, system or system sub-assembly for eventual sale to the marketplace by the OEM.

Customer – At a minimum, this will be the OEM. If a CM is involved in the manufacturing process, then there are two customers in the business transaction, the OEM and the CM. Even if the CM is the party placing the orders, the primary customer is the OEM, followed by the CM. If a distributor is involved in the supply chain, there could be a third customer in the business transaction.

Designer – The party doing the device selection as part of an overall system or sub-system design. The most common scenario would be the OEM as the designer, but it is possible that a CM might do the design on behalf of the OEM.

KGD – Known Good Die (defined in Product Test Methodology section above).

LGD – Lattice Good Die (defined in Product Test Methodology section above).

OEM – Original Equipment Manufacturer: The final consumer of the Die product. Die product is incorporated into the OEM's end products for sale to the marketplace.

OPN – Ordering part number.

Wafer Map – Electronic file identifying good vs bad die on a given wafer.

Business Engagement Process

1. Designer identifies candidate Die from the Lattice Die sale offering.
2. Designer evaluates device-specific data sheet, Lattice Die Sale Data Sheet, Pin Tables and Die Dimensional Data to confirm that the candidate Die will meet the performance and dimensional constraints of the design.
3. Designer solicits a price quotation from a Lattice Sales Representative or authorized Distributor.
4. Lattice Sales Representative/Distributor to quote a per-Die price along with an average Die per wafer quantity. This quantity represents the minimum order quantity and order increment quantity.
5. Customer(s) signs the Lattice Die Sale Data Sheet Acknowledgment form located at the back of the Lattice Die Sale Data Sheet.
   a. At a minimum, this will be the OEM. If a CM is also involved in the manufacturing process, the CM will also need to sign the Acknowledgement.
   b. If the order is being placed through a Lattice authorized distributor, the distributor must also sign the Acknowledgement.
6. Customer identifies a minimum of one email address to be the recipient of any Wafer Map(s).
   a. Can send Wafer Map(s) to the OEM, CM and/or Distributor.
   b. Record email address(es) on the Acknowledgement Form at end of this data sheet.
7. Customer places order with a Lattice Sales Representative or Lattice authorized Distributor in increments of the quoted average Die per wafer.

8. Lattice sells Die to OEMs through one of two sales channels:

   a. Direct – For those OEMs with a pre-existing OEM relationship with Lattice. Such sales will be directed though a Lattice Authorized Sales Representative.

   b. Distribution – Through a Lattice authorized distributor. For the distributor channel, terms and conditions of sale must be established between the customer and the distributor, however, the expectation is that the customer will have a substantially similar experience with either channel.

   c. Lattice will also sell Die to CMs as long as the CM is working in direct support of an identified OEM end-equipment program.

   d. Lattice will not sell Die to a CM for subsequent sale to the broad market. There must always be a clearly identified OEM relationship.

9. Pre-Programmed Die – Lattice has the capability to program a customer-specific functional pattern into the Die as part of the wafer-level test flow. This capability would pertain to Non-Volatile products (See Table 1) only. Contact your Lattice Sales Representative for details.

Terms and Conditions of Sale

In these Terms and Conditions of Sale, “Lattice” means Lattice SG. Pte. Ltd., the seller of Products. “Customer”, “OEM” and “CM” have each been defined above in the Definition of Terms Section. “Products” means the applicable unpackaged Die products, described in this data sheet. Unless otherwise set forth herein, Lattice’s Terms of Sale located at:

http://www.latticesemi.com/~/media/Documents/Policies/LatticeTermsandConditions.PDF?document_id=6726

apply to Customer’s purchase of Products directly from Lattice. For Products purchased from a Lattice authorized distributor, these Terms and Conditions of Sale, together with any additional terms and conditions for the purchase of Products agreed upon between Customer and the Lattice authorized distributor will be applicable.

1. Orders

Customer must place orders in increments of the quoted, average good Die per wafer.

2. Shipment

At the time of shipment, Lattice will modify the “ordered” quantity to match the actual number of good Die on the specific wafer(s) being shipped to the Customer.

   a. The actual quantity of Die on a given wafer will be +/- 10% of the quoted average good Die per wafer.

   b. The customer will only be invoiced for the exact quantity of KGD or LGD Die shipped. The order will be deemed to be shipped in full once the quantity adjustment has been made and the wafer(s) shipped by Lattice.

3. Cancellation and Rescheduling of Orders

Cancellation: Customer acknowledges and agrees that Products purchased hereunder are custom products. As such, all orders for Products placed by Customer are non-cancellable and non-returnable.

Rescheduling: Customer may reschedule shipment of Products by giving Lattice written notice at least sixty (60) days prior to the scheduled shipment date. Orders may only be rescheduled once and for no more than ninety (90) days delay from the original shipment date.

4. OEM Certification

Customer certifies that Products will be purchased by Customer for use by Customer:

as a contract manufacturer (CM) for an original equipment manufacturer (OEM), and will be utilized by Customer with significant value added and as part of a system or subsystem assembly manufactured by Customer, that will be distributed to the original equipment manufacturer in the regular course of customer's business; or

as an original equipment manufacturer (OEM) and will be utilized by Customer with significant value added and as part of a system or subsystem assembly by Customer, that will be distributed in the regular course of Customer's business.

Customer may not resell Products in the original unpackaged (wafer or singulated Die) form. Upon Lattice's request, Customer will furnish to Lattice evidence of compliance with the provisions of this section.

5. Warranty

THE PARTIES UNDERSTAND THAT CUSTOMER IS PURCHASING SEMICONDUCTOR DEVICES THAT ARE NOT FINISHED OR FULLY ENCAPSULATED AND THEREFORE ALL PRODUCTS ARE DELIVERED "AS IS." LATTICE MAKES, AND CUSTOMER RECEIVES, NO WARRANTIES OR CONDITIONS, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE, AND LATTICE SPECIFICALLY DISCLAIMS ANY IMPLIED WARRANTIES OR CONDITIONS OF MERCHANTABILITY, SATISFACTORY QUALITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. No agent, employee, or representative of Lattice has any authority to bind Lattice to any affirmation, representation, or warranty relating to the Products.

CUSTOMER ACKNOWLEDGES THAT LATTICE MAKES NO RECOMMENDATION REGARDING THE SUITABILITY OF PRODUCTS SOLD HEREUNDER FOR ANY PARTICULAR USE OR APPLICATION. CUSTOMER ASSUMES FULL RESPONSIBILITY FOR THE SELECTION OF SUCH PRODUCTS AND FOR THE DESIGN, DEVELOPMENT, AND TESTING OF ANY PRODUCTS INTO WHICH PRODUCTS SOLD HEREUNDER MAY BE INCORPORATED. CUSTOMER FURTHER ASSUMES FULL RESPONSIBILITY FOR ANY CONSEQUENCES THAT MAY RESULT DIRECTLY OR INDIRECTLY FROM USE OF PRODUCTS SOLD HEREUNDER.

6. Technical Support

Lattice will provide no specific, ongoing technical support for the use of Products in Customer-specified applications. Technical analysis of the operation of Die shipped by Lattice, in packaged configurations determined by Customer, is solely the responsibility of Customer. Technical assistance provided by Lattice to Customer is at the sole discretion of Lattice.

7. No Right to Manufacture/Copy

The Products are sold by Lattice subject, in every case, to the condition that such sale does not convey any license, by implication, estoppel, or otherwise, to manufacture, duplicate, or other¬wise copy or reproduce the Products, through reverse engineering or any other means. Customer agrees to take appropriate steps with its customers, suppliers and contractors, as Lattice may request, to inform them of and assure their compliance with the restrictions contained in this section. In addition, Customer shall not use or sell the Products in packaged form to compete with Lattice.

ACKNOWLEDGEMENT

(Signed by OEM AND CM and/or Distributor, if used)

By signing this acknowledgement, each party (identified below) hereby acknowledges and accepts that the purchase of Products is subject to all terms and conditions set forth in this data sheet. This acknowledgement applies to all shipments of the Ordering Part Number listed below.

OEM Name/Location: _____

OEM Project Name: _____

Die Ordering Part Number: _____

CM Name/Location (if applicable): _____

Authorized Distributor Name (if applicable): _____

Authorized OEM Representative Signature:

Name: _____

Position/Title: _____

Signature: _____

Date: _____

Wafer Map Email Address[1]: _____

Authorized CM Representative Signature (If applicable):

Name: _____

Position/Title: _____

Signature: _____

Date: _____

Wafer Map Email Address[1]: _____

Authorized Distributor Representative Signature (If applicable):

Name: _____

Position/Title: _____

Signature: _____

Date: _____

Wafer Map Email Address[1]: _____

1. A minimum of one email address must be provided on this form to receive wafer map(s).

Revision History

Date	Version	Section	Change Summary
March 2015	1.0	All	Initial release.