Cable Configuration (CC), Power Delivery (PD) and Display Port (DP) Demo for USB Type-C Demo Kit V2 User Guide

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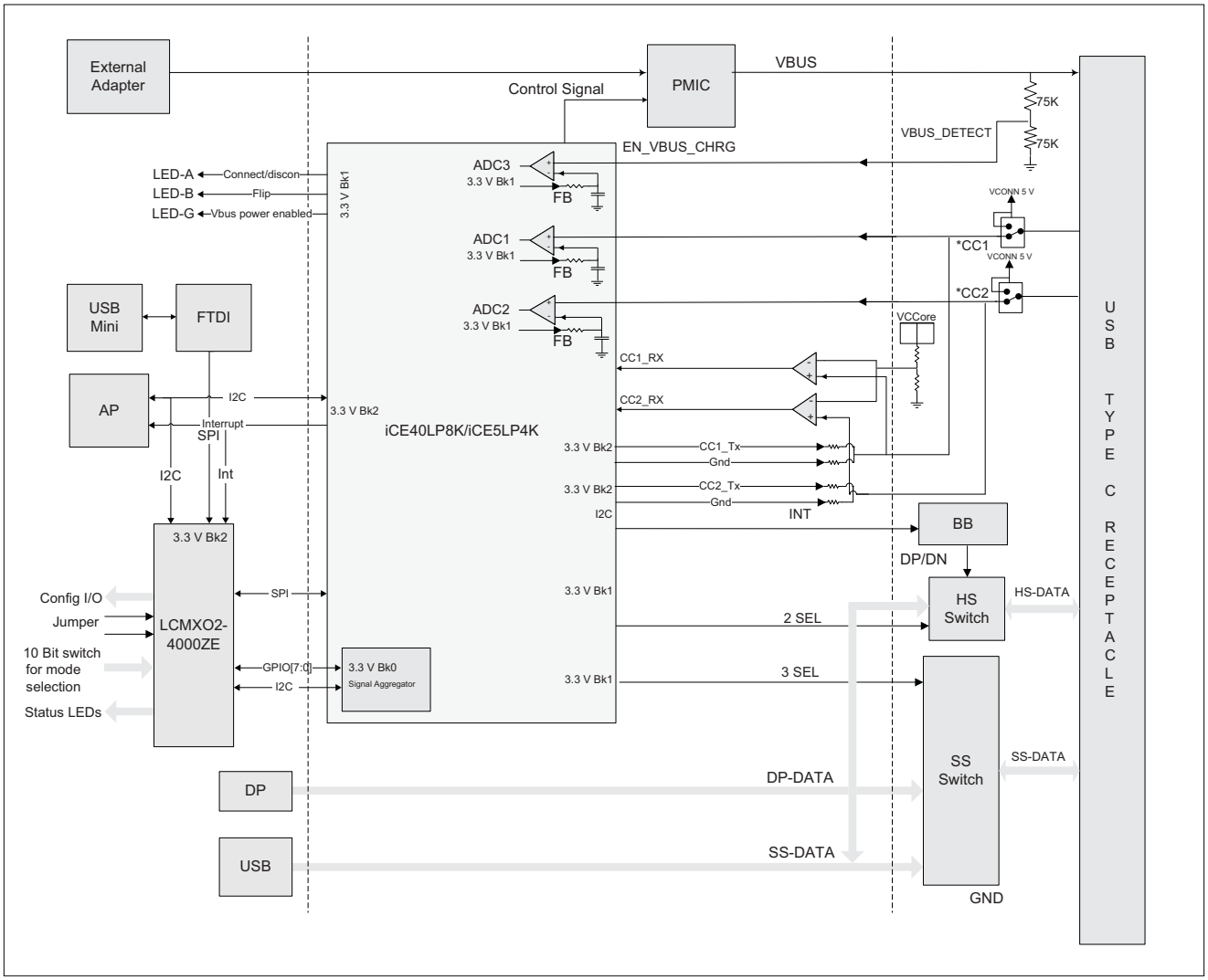
Introduction

This user guide describes the design and procedure for Cable Configuration (CC), Power Delivery (PD) and Display Port (DP) demo on USB Type-C Demo Kit V2 Board. Figure 1 shows the block diagram of USB Type-C Power Delivery solution, which is implemented on the board to demonstrate the features. The USB Type-C Demo Kit V2 Board is referred to as "demo board" in this document.

Figure 1. USB Type-C Power Delivery Block Diagram



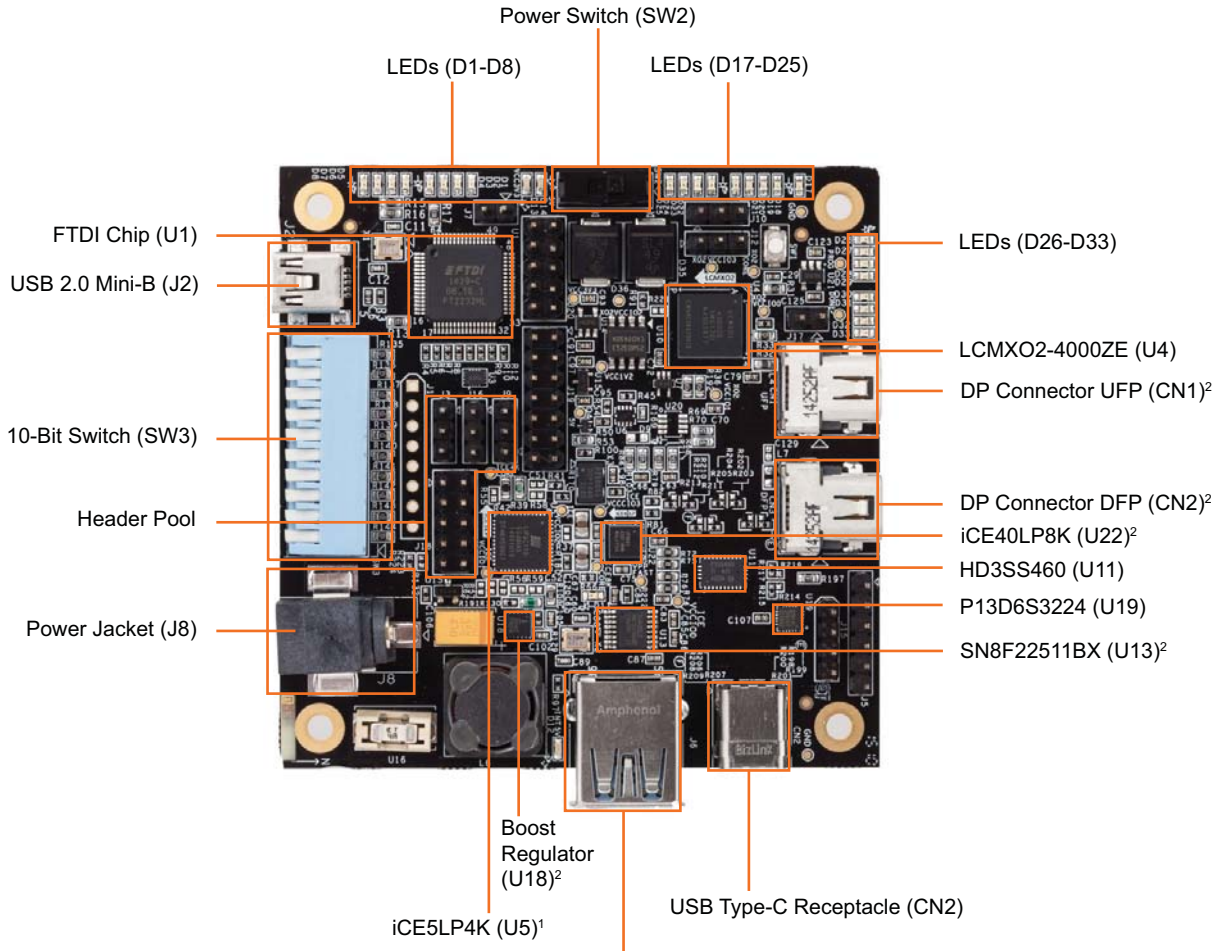
Two variations of the demo board are available. One is built around an iCE40 device and the other one uses an iCE40 Ultra device. Both types of board support dual role port (DRP) operation. DRP devices can act as a downstream facing port (DFP) or an upstream facing port (UFP).

The following three demos are available:

- Demo 1: DRP and Display Port Alternate Mode Demo with iCE40 Device
- Demo 2: DRP and Lattice Alternate Mode Demo with iCE40 Device
- Demo 3: DRP Demo with iCE40 Ultra Device

Figure 2 shows the top view of the demo board. Refer to EB99, USB Type-C Demo V2 Kit Board User Guide for a detailed description and schematics of the board.

Figure 2. Top View of Demo Board



Notes:
1. iCE5LP4K-USBC EVN Only
2. iCE40LP8K-USBC EVN Only

Table 1 describes the key components present on the board.

Table 1. Demo Board Key Components

COMPONENTS	DESCRIPTION
USB 2.0 Mini-B (J2)	USB Mini connector is used to supply 5 V power, program the device on board, and data logging.
Power Jack (J8)	For connecting external power adapter to supply 5 V
Mini DP Connector (CN1,CN3)	Mini display port source and sink
USB Type-C Receptacle (CN2)	USB Type-C receptacle which acts as power and data source and sink
USB Type-A Receptacle (J6)	USB data source and sink
FTDI Chip (U1)	Used for programming through USB interface
LCMXO2-4000ZE (U4)	Programming MUX glue logic, aggregator signal generator/receiver, and LED control
iCE40LP8K (U22)	PD manager and CC-PD PHY
iCE5LP4K (U5)	PD manager and CC-PD PHY
HD3SS460 (U11)	SS/DP switch which supports display port and USB super speed signaling
PI3D6S3224 (U19)	High speed MUX which supports USB2.0 data switching
SN8F22511BX (U13)	Billboard device which is exposed to the host when alternate mode fails
Power Switch (SW2)	Controls board power- on/off switch
10-Bit Switch (SW3)	General purpose input and config/programming switch
LEDs D1-D8	Aggregator status LED
LEDs D17-D32	USB Type-C PD status LED
Headers	Probing and external interface

The board is based on either an iCE40 (iCE40LP8K) or an iCE40 Ultra (iCE5LP4K) device depending on the ordering part number. The supported features for the different part numbers are listed below:

- **iCE40LP8K** – The iCE40LP8K Package supports all the features listed in the Features Supported by the Demo Board section.
- **iCE5LP4K** – The iCE5LP4K Package supports all the features listed in the Features Supported by the Demo Board section except the following:
  - — Data Role Swap
  - — Power Role Swap
  - — Alternate Mode (DP)
  - — Aggregator
  - — 20 V Support

Features Supported by the Demo Board

- Dual Role Port (DRP)
- Attach/Detach
- Flip Mode
- BMC (Biphase Mask Coding) and Power Delivery (PD) Contract
- Multiple Sink Requests
- Data Role Swap
- Power Role Swap
- Dead Battery
- Superspeed Signaling
- Alternate Mode (DP)
- Aggregator
- 20 V Support

Demo Requirements

- Demo Boards (2)
- Type-C to Type-C Cable
- Lattice Diamond® Programmer version 3.2 or higher
- USB 2.0 Type A to Type-B mini cable
- USB standard Male to Male cable
- Mini DP Male to Male cable
- Mini DP Male to DP Male cable
- USB 3.0 memory stick
- Power adapters
- Laptop with mini DP output (1), DP display (1)
- Bitstreams for the Lattice device
- Tera Term (similar terminal) application or Lattice I2C utility

Default Board Header Settings

Table 2 shows the header options and their recommended default settings for normal operation of the Demo Board.

Table 2. Headers and Test Connectors

Part	Description	Setting Options	Default Setting
J1	External JTAG I/F		
J3	JTAG/SPI Selection	1-2 (SPI), 2-3 (JTAG)	JTAG
J16	JTAG/I^2C Selection	1-2 (JTAG), 2-3 (I^2C)	JTAG
SW1	MachXO2 Reset Switch		
J17	Jumper for DP Power	Open-Off, Short-On	Open
J5	BB Device Programmer I/F		
SW2	Board Power Switch	Left-On, Right-Off	Right
J7	VBUS Sink Connector	Open-Off, Short-On	Open
SW3	General Purpose Input Switch		
J9	USB Role Selection	1-2 (UFP), 2-3 (DFP)	Open
J10	MachXO2 I/O HIZ Enable	1-2 (Enable), 2-3 (Disable)	Open
J15	For Testing/Probing		
J12	MachXO2 I/O Direction Input	1-2 (Input), 2-3 (Output)	Open
J20	For Testing/Probing		
J18	External AARDVARK I/F		
J19	External AGG Inputs		

Demo Board Status LEDs

Table 3 provides the descriptions of status LEDs for each demo, LED colors and net names.

Table 3. Status LEDs

LED	Schematic NET	Demo 1 Description	Demo 2 Description	Demo 3 Description	Color
D1	AGG_LED1	PDO1	AGGR STROBE DATA	NA	Green
D2	AGG_LED2	PDO2	AGGR STROBE DATA	NA	Green
D3	AGG_LED3	PDO3	AGGR STROBE DATA	NA	Green
D4	AGG_LED4	PDO4	AGGR STROBE DATA	NA	Green
D5	AGG_LED5	PDO5	AGGR I^2C DATA	NA	Green
D6	AGG_LED6	PDO6	AGGR I^2C DATA	NA	Green
D7	AGG_LED7	NA	AGGR I^2C DATA	NA	Green
D8	AGG_LED8	NA	AGGR I^2C DATA	NA	Green
D9	4KDONE	CONFIG SUCCESS	CONFIG SUCCESS	CONFIG SUCCESS	Blue
D11	CDONE	CONFIG SUCCESS	CONFIG SUCCESS	CONFIG SUCCESS	Red
D17	STATUS_LED1	Cable Attached	Cable Attached	Cable Attached	Blue
D18	STATUS_LED10	Flip	Flip	Flip	Blue
D19	STATUS_LED11	Source/Sink	Source/Sink	Source/Sink	Blue
D20	STATUS_LED2	PD contract established	PD contract established	PD contract established	Blue
D21	STATUS_LED12	DFP/UFP	PDO1	PDO1	Green
D22	STATUS_LED3	NA	PDO2	NA	Green
D23	STATUS_LED13	NA	PDO3	NA	Green
D24	STATUS_LED4	ALT_MODE	ALT_MODE	NA	Green
D25	STATUS_LED14	NA	NA	NA	Green
D26	STATUS_LED5	PR SWAP	NA	NA	Red
D27	STATUS_LED6	DR SWAP	NA	NA	Red
D28	STATUS_LED15	SS POL	SS POL	NA	Blue
D29	STATUS_LED16	SS SEL	SS SEL	NA	Blue
D30	STATUS_LED7	SS Enable	SS Enable	NA	Yellow
D31	STATUS_LED8	VBUS 5 V	VBUS 5V	VBUS 5V	Yellow
D32	STATUS_LED17	VBUS 20 V	NA	NA	Blue
D33	STATUS_LED9	BOOT LED	BOOT LED	BOOT LED	Yellow

Device Configuration

The sections below explain the programming/configuration procedure for each device in the Demo Board. The procedure applies to both iCE40LP8K and iCE5LP4K based boards.

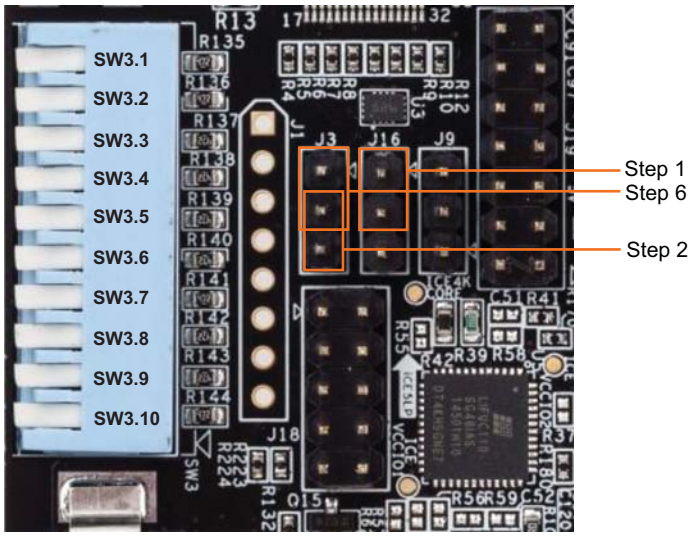
Programming and Configuration Settings

Demo Board supports the programming of FPGA devices from the flash device or directly through FTDI chip using Mini USB (J2) Connector. The programming mode and device selection are set by dual in-line package (DIP) switches SW3. Table 4 shows the switch settings for different programming modes and device selections. Refer to Figure 3 for the jumper and switch settings, and the programming sequences.

Table 4. Programming Mode Selection

Device	Operation	Mode	Jumper Position		DIPSW (SW3) Position	
			J16	J3	SW3.1	SW3.2
MachXO2	Program/Configure	JTAG	1-2	3-2	Up	Down
iCE40 CRAM	Program/Configure	SPI	1-2	1-2	Down	Down
iCE40 Flash	Program/Configure	SPI	1-2	1-2	Down	Up
(All)	Boot	—	3-2	—	Up	Up

Figure 3. Header and Switch Setting for Programming

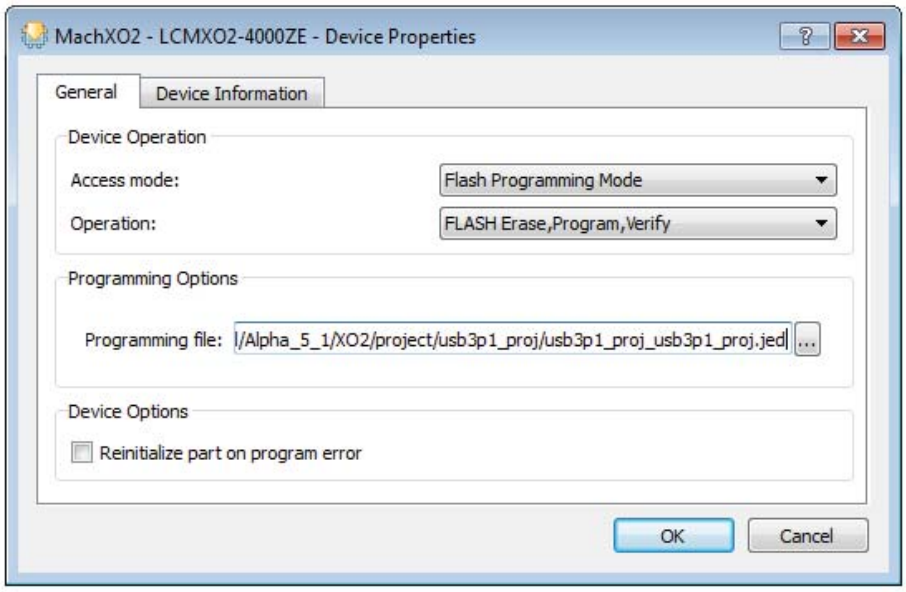


Programming Sequence

To program the board:

1. Connect the jumper between J16.1 and J16.2.
2. Connect the jumper between J3.2 and J3.3.
3. Power on the board.
4. Program the MachXO2 device. Refer to Figure 4 for the programming settings.

Figure 4. MachXO2 Flash Programming Settings



5. Remove the jumper between J3.2 and J3.3
6. Connect the jumper between J3.1 and J3.2.
7. Program the iCE40 Flash.

   a. For iCE40LP8K: Program iCE40LP8K Flash. Refer to Figure 5 for the programming settings. LED D11 glows after successful programming.

   b. For iCE5LP4K: Program iCE5lP1K Flash. Refer to Figure 6 for the programming settings. LED D9 glows after successful programming.

Figure 5. iCE40LP8K Serial Flash Programming Settings

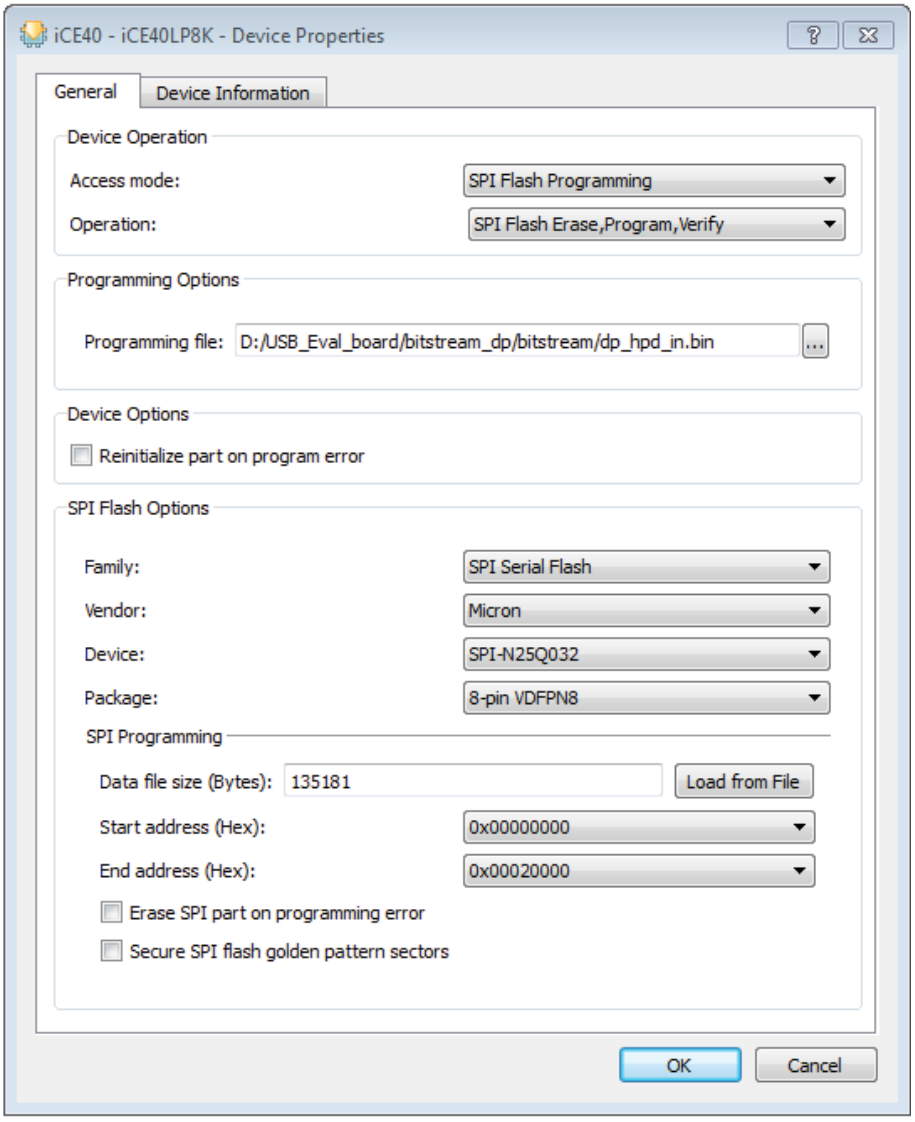
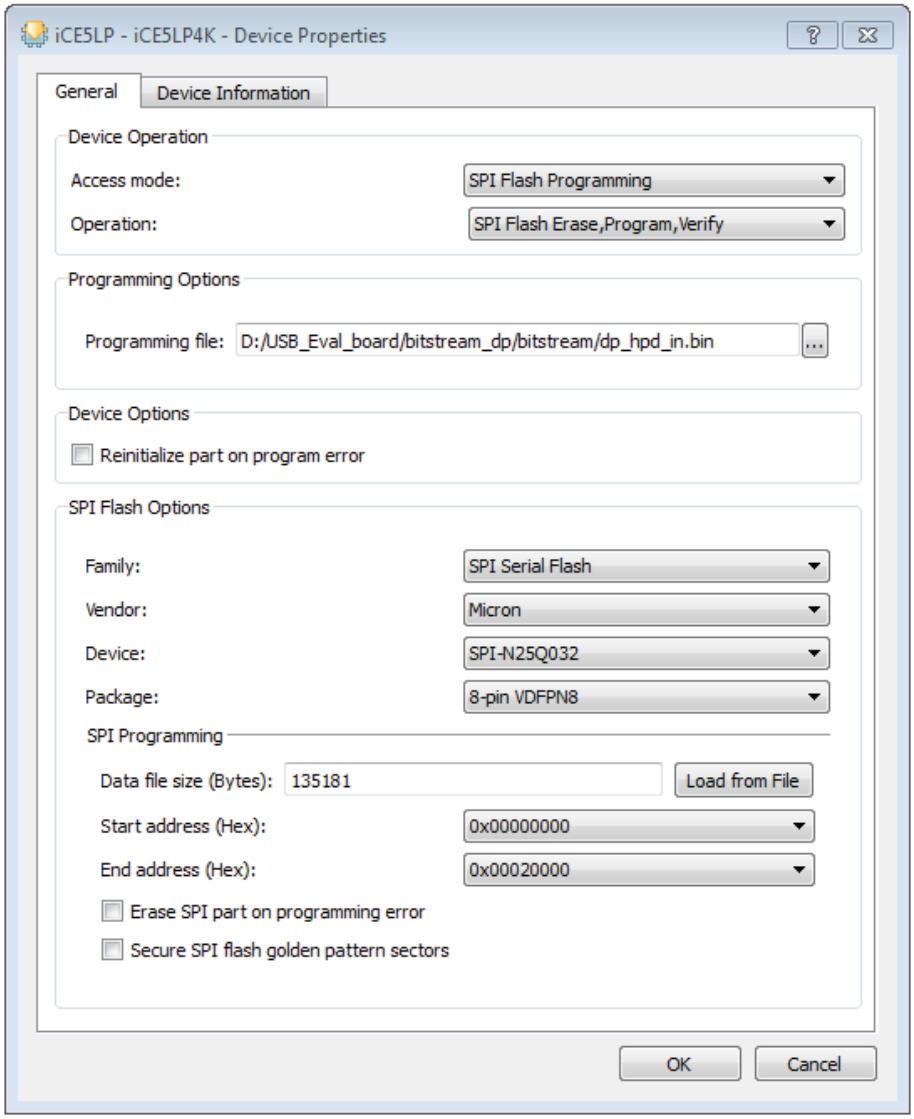


Figure 6. iCE5LP4K Serial Flash Programming Settings



8. Set DIP switch SW3 in boot mode after successful programming. Refer to Table 4 for boot mode.

Setting Up the Board for Demos

To set up the board after programming the devices:

1. Set SW3.1 and SW3.2 Up to put the board in boot mode.
2. Power on both boards. Note that at least one of the boards must be powered by a 5 V DC supply through connector J8. The other board can be powered either by a power supply or through a USB mini connector J2. Make sure the boot LED D33 is turned ON.
3. Set SW3.4 and SW3.5 to put the board in the desired mode (DRP, DFP or UFP). Refer to Table 5 for the settings.
4. Leave the jumper J7 open for normal operation. (J7 needs to shunted only for the dead battery demo.)

Table 5. DRP/DFP/UFP Selection[1]

Port Role	SW3.4	SW3.5
DRP	UP	NA
DFP	Down	UP
UFP	Down	Down

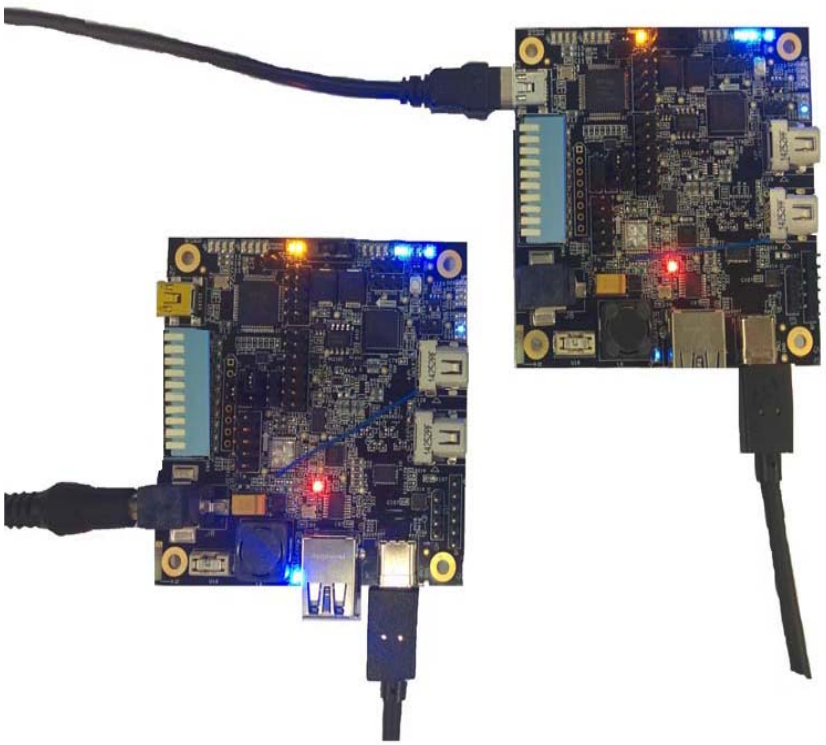
1. Only applicable for Demo1 and Demo 2

Demo 1: DRP and Display Port Alternate Mode Demo with iCE40 Device

Figure 7 shows the test setup for testing the different USB Type-C power delivery features. Demo Board supports dual role port (DRP) which act as either Downstream Facing Port (DFP) or Upstream Facing Port (UFP). When two DRP boards are powered and connected through a Type-C cable, one board takes the role of DFP and the other UFP automatically.

Most of the demos described here has both boards set as DRP. You can also set one of the boards as DFP or UFP. The boards can be set to any role by setting the switches as shown in Table 5.

Figure 7. USB Type-C Feature Test Setup



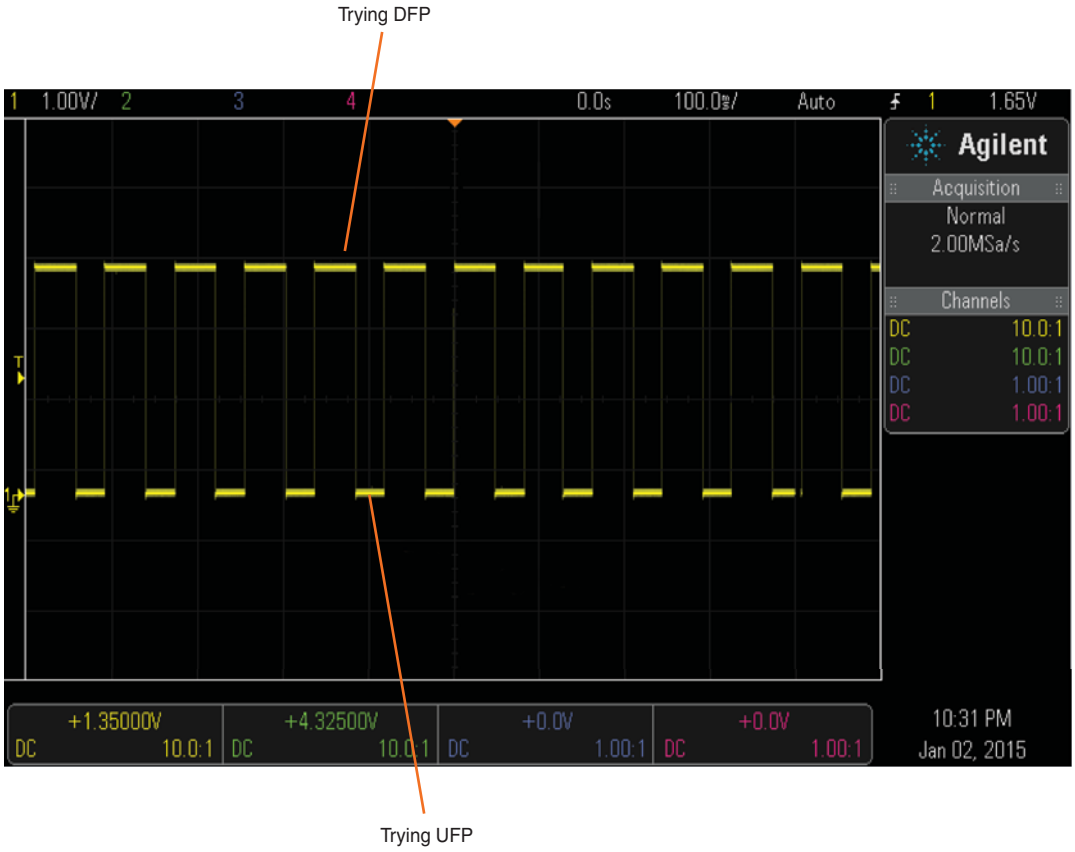
Before Cable Attach

To observe the port behavior before cable attach:

1. Set the DIP switch SW3.4 Up, to enable DRP mode.
2. Probe J15.3 or J15.4 for the CC lines to verify if the board is acting as DRP. When the board is functioning as DRP and when a cable is not attached, the voltage on CC lines toggle up and down, indicating that the DRP trying to become a DFP or a UFP.

Refer to Figure 8 for the waveforms.

Figure 8. Dual Role Port Behavior On CC Lines



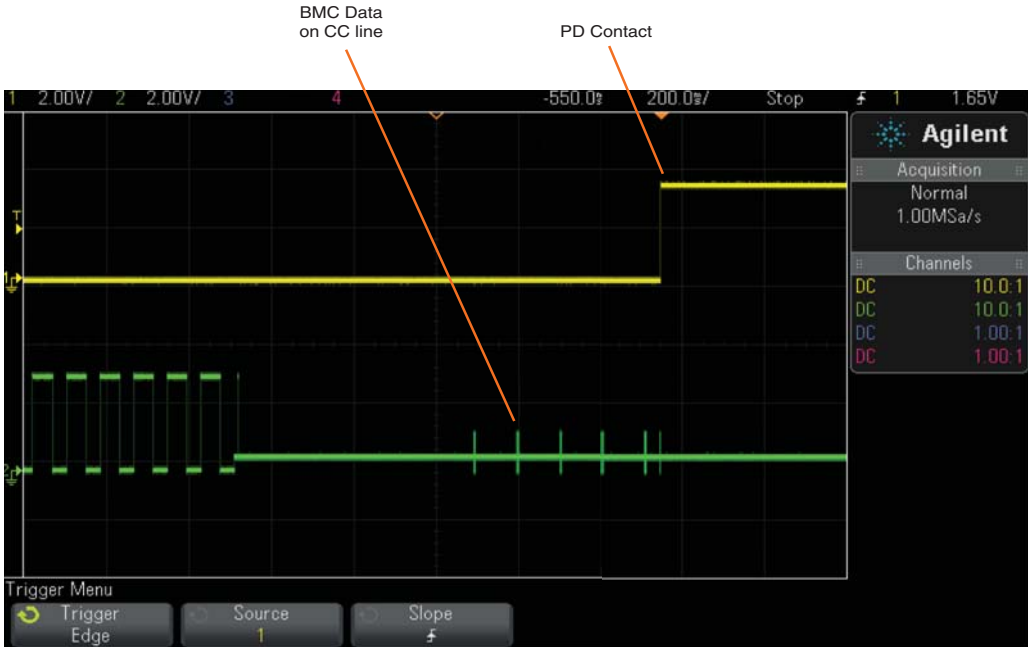
Cable Detection (Attach and Detach)

To test cable attach and detach conditions:

1. Connect two DRP boards using USB Type-C cable in Normal Mode. LED D17 glows to indicate the boards are connected with Type-C cable. LED D20 glows to indicate the PD contract is established and can be probed on PD_CONTRACT(J15.2).
2. Probe CC1 or CC2 to see the behavior and voltage during UFP attaching with DFP as shown in Figure 9.
3. Unplug Type-C cable from any one of the boards. LED D17 turns off to indicate the Type-C cable is detached.
4. Probe on either CC1(J15.3) or CC2 line (J15.4).

Refer to Figure 9 for the waveforms.

Figure 9. CC Waveform (UFP Attaching to DFP)



Flip Mode

To demonstrate cable flip mode:

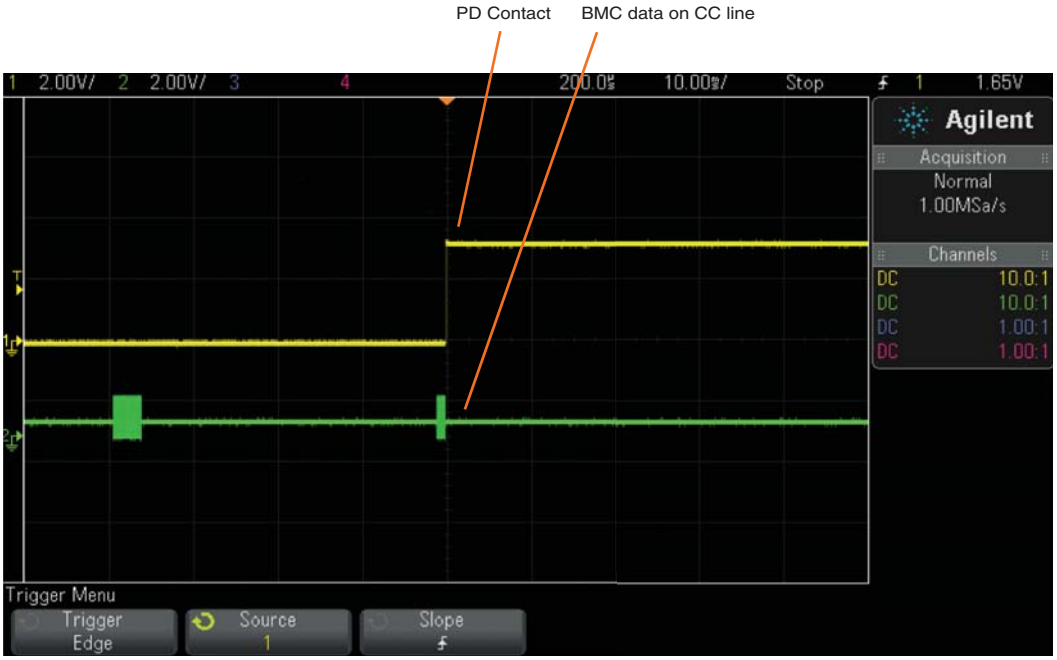
1. Flip the Type-C cable on one of the boards. LED D18 glows on that board to indicate that the Type-C cable is flipped.
2. Flip the Type-C cable on the second board. LED D18 glows on that board to indicate that the Type-C cable is flipped. LED D20 glows to indicate that the PD contract is established.
3. Probe either CC1 (J15.3) or CC2 line (J15.4) for the activities on CC lines. Refer to Figure 8 for the waveforms.
4. Unplug Type-C cable from any of the boards. LED D17 turns off to indicate cable is detached.

BMC and PD Contract

To view BMC communication between the boards:

1. Connect an oscilloscope probe to CC1 (J15.3) in Normal mode or CC2 (J15.4) in Flip mode. PD contract can be probed on PD_CONTRACT(J15.2) header.
2. On Oscilloscope, set the trigger for on PD_CONTRACT(J15.2) rising edge.
3. Connect the boards in either Normal mode or Flip mode by using Type-C cable. When a successful connection is established, BMC communication and PD contract can be seen on the Oscilloscope as shown in Figure 10.

Figure 10. BMC and PD Contract



4. Probe on either CC1(J15.3) or CC2 line (J15.4) to see BMC communication as shown in Figure 10.

Source Capabilities and Sink Requests

The source capabilities for the demo design has two power data objects (PDOs) as defined in Table 6.

Table 6. Supported Source PDOs

Source PDOs	iCE5LP4K	iCE40LP8K
5 V, 0.9 A	Yes (PDO1)	Yes (PDO1)
20 V, 0.8 A	NA	Yes (PDO2)

The sink PDOs for the design are shown in Table 7.

Table 7. Supported Sink PDOs

Sink PDOs	iCE5LP4K	iCE40LP8K
5 V, 800 mA	NA	Yes (PDO1)
5 V, 900 mA	Yes (PDO1)	NA
7 V, 800 mA	NA	Yes (PDO2)
9 V, 800 mA	NA	Yes (PDO3)
12 V, 800 mA	NA	Yes (PDO4)
18 V, 800 mA	NA	Yes (PDO5)
20 V, 800 mA	NA	Yes (PDO6)

The board acting as UFP can request for a sink voltage from any one of the sink PDOs.

To make a new power request:

1. Set the DIP switches SW3.7, SW3.8, SW3.9 corresponding to the sink PDO object. Refer to Table 8.
2. Toggle SW3.6 to initiate the request.
3. LED (D1 - D6) corresponding to the negotiated PDO lights up. Refer to Table 1.

If the request is accepted by DFP, an LED corresponding to the newly accepted power profile lights up.

Table 8. Sink PDOS Selection[1]

Sink PDOs	V, I value	DIP Switch Position		
		SW3.7	SW3.8	SW3.9
PDO1	5 V, 800 mA	Up	Down	Down
PDO2	7 V, 800 mA	Down	Up	Down
PDO3	9 V, 800 mA	Up	Up	Down
PDO4	12 V, 800 mA	Down	Down	Up
PDO5	18 V, 800 mA	Up	Down	Up
PDO6	20 V, 800 mA	Down	Up	Up

1. SW3.6 – Change the level of SW3.6 switch to initiate new PDO request (Only applicable for Demo 1.)

Table 9. Swap Selection

SW3.7	SW3.8	Swap Function
Down	Down	Data Role Swap
Up	Down	Power Role Swap
Down	Up	Hard Reset
Up	Up	Exit VDM Mode

1. SW3.10 – Change the level of SW3.10 switch to initiate SWAP (Only applicable for Demo 1.)

Data Role Swap

The data roles can be swapped by the port partners dynamically. Data Role Swap can be initiated using on-board switches shown in Table 9. When the boards are working in normal or flipped mode, it can swap their Data roles from DFP to UFP or UFP to DFP dynamically. Either DFP or UFP can initiate the Data Role Swap. As only the data roles change, the power role as indicated by source LED D19 is not changed.

To initiate the Data Role Swap on the board:

1. Set the DIP switch SW3.7 and SW3.8 Down to enable the Data Role Swap.
2. Change the DIP switch SW3.10 level, to initiate Data role swap.

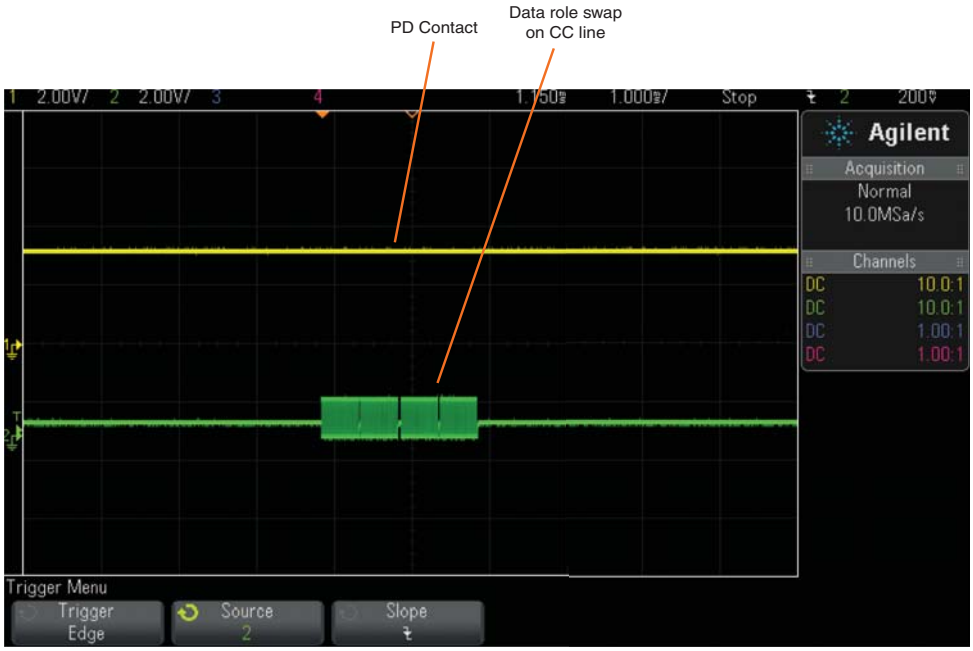
Note: Before initiating the "Data Role" swap from DFP or UFP device, the devices should exit from Alternate (ALT) mode. To exit from ALT mode, follow the steps given below.

1. *On DFP board, set the DIP switch SW3.7 and SW3.8 UP to enable the Exit VDM mode settings.*
2. *On DFP board, change the DIP switch SW3.10 level to initiate Exit VDM mode.*

LED D27 glows to indicate that a Data Role Swap is initiated and successful.

BMC data can be probed on CC1 in normal mode and CC2 in flip mode. PD contract established can be probed on PD_CONTRACT (J15.2) header. Refer to Figure 11 for the data activity on the CC line on data swap.

Figure 11. Data Role Swap



Power Role Swap

The power roles (source or sink) can be swapped by the port partners dynamically. Power Role Swap can be initiated using on board switches shown in Table 9. Either DFP or UFP initiates the Power Role Swap and changes only Power roles. Data role remains unchanged. Source LED D19 swaps between the boards based on the role that is negotiated. The board with LED D19 turns ON, acts as DFP and board with LED D19 turns OFF, acts as UFP.

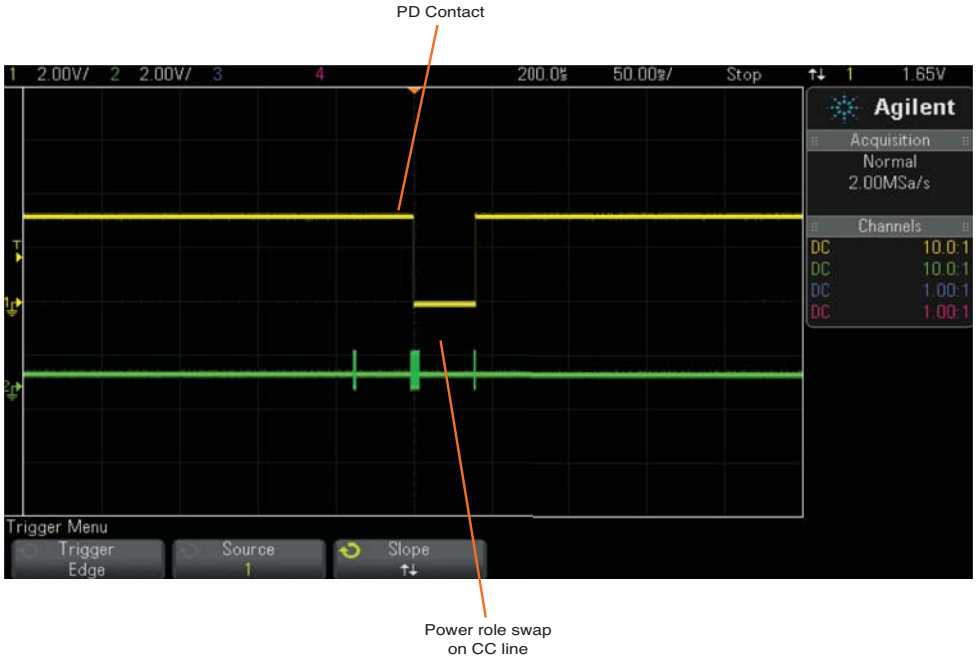
To initiate the Power Role Swap on the board:

1. Set the DIP switch SW3.7 Up and SW3.8 Down to enable the Power Role Swap.
2. Change the DIP switch SW3.10 level, to initiate Power role swap.

LED D26 glows to indicate that a Power Role Swap is initiated and successful.

BMC data can be probed on active CC lines. The PD contract established can be probed on PD_CONTRACT(J15.2) header. Refer to Figure 12, for waveforms of the data activity on the CC line on power swap.

Figure 12. Power Role Swap

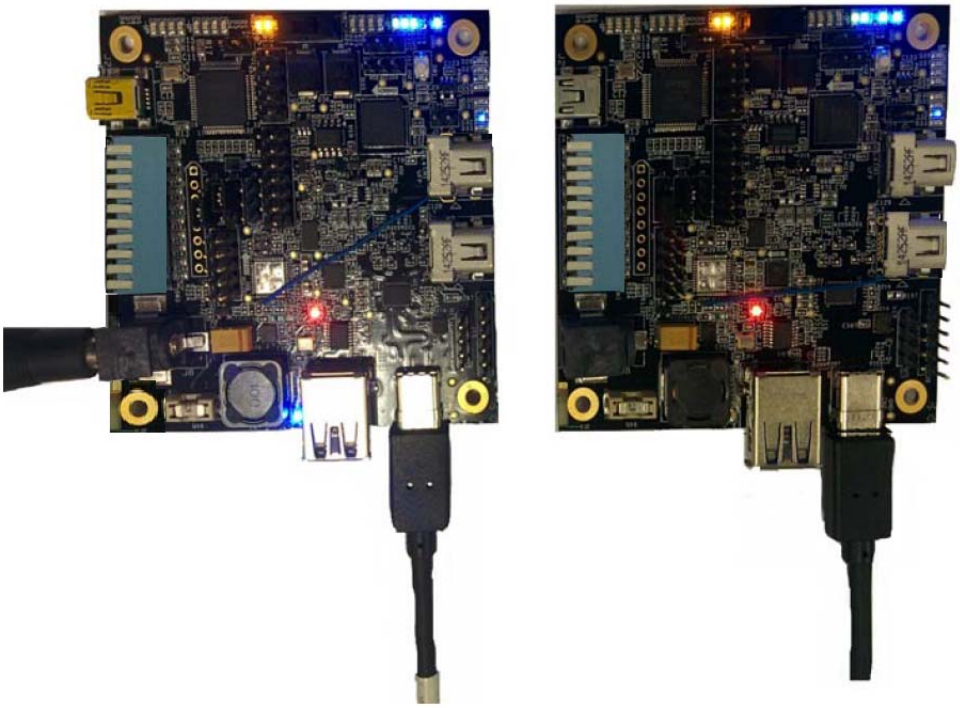


Dead Battery

Dead battery feature is demonstrated by using one powered board and one dead battery (unpowered) board. The powered board will power and bring-up the dead battery board. Figure 13 shows the test setup for testing dead battery condition. Dead battery test supports only 5 V.

Caution: Care must be taken during dead battery test. Specifically, you cannot create a dead battery condition when a 20 V power contract is in place. You also should not try to negotiate a 20 V contract when one of the boards has a dead battery. These conditions will damage the board. To prevent damage to the board, remove the Type-C cable between the boards first before removing power from the dead battery board.

Figure 13. Dead Battery Demo Setup



To perform dead battery demo:

1. Keep all the switches (SW3) UP.
2. Leave J7.1 and J7.2 open on the board that is going to act as the power sourcing device and DFP.
3. Short J7.1 and J7.2 on the dead battery board to make it a sink and UFP.
4. Connect the unpowered board with the powered board using Type-C cable.

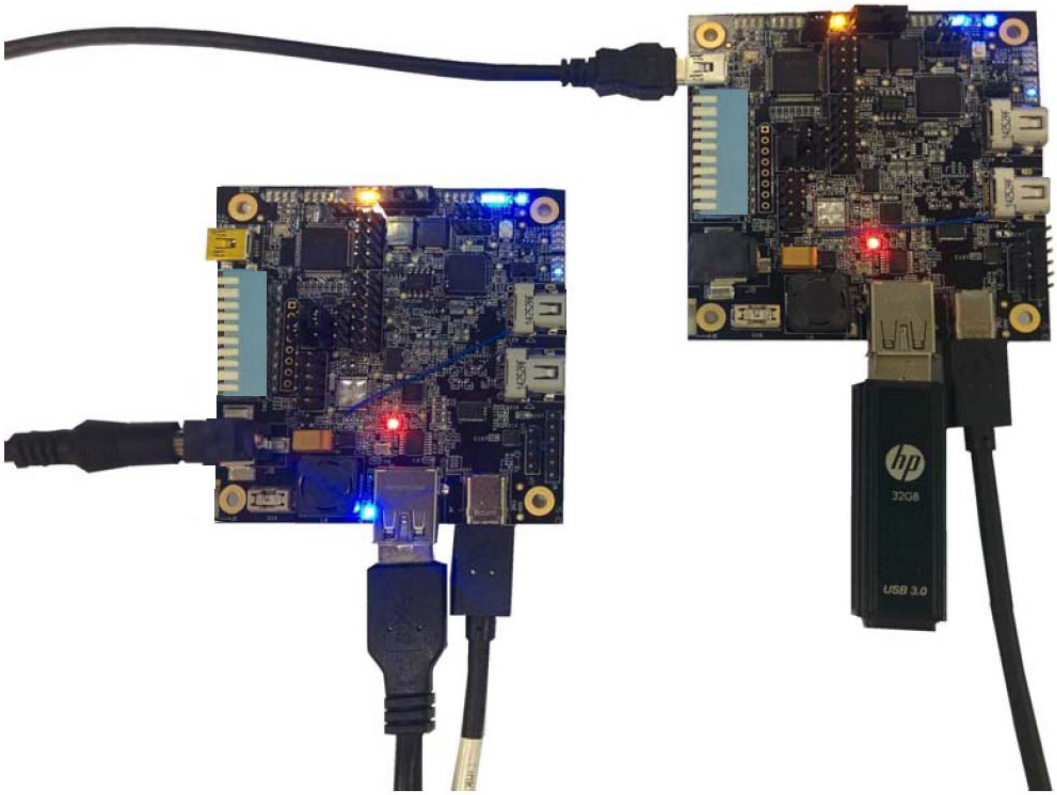
The powered board detects the cable attached and act as DFP. LED D17 glows to indicate partner attached and LED D19 glows to indicate that it is sourcing power (DFP) to the unpowered board. The dead battery board comes up as a UFP-Sink device. The powered board acts as DFP and the unpowered board acts as UFP. The unpowered board LED D19 glows to indicate that it is sinking power from the powered board. LED D20 glows to indicate the PD contract is established.

BMC data can be probed on active CC lines. PD contract established can be probed on PD_CONTRACT(J15.2) header. Refer to Figure 10 for the waveforms.

SS/HS Switch Muxing and Signaling

Figure 14 shows the test setup for HS/SS switch muxing and signalling.

Figure 14. HS Switch Muxing Test Setup



To test HS/SS switch muxing:

1. Connect a USB 3.0 male to male cable from a computer to one demo board (J6).
2. Connect a Type-C cable between the demo boards in normal mode.
3. Connect a USB 3.0 memory stick to the second board (J6).
4. Access data from the memory stick from a computer.
5. To test the flip mode, plug out the USB 3.0 memory stick.
6. Disconnect the Type-C cable and connect it again in flip mode.
7. Plug in the USB 3.0 memory stick.
8. Access data from the memory stick from a computer.

To verify the speed of the USB connection, you may use an application such as *USB Tree* as shown in Figure 15.

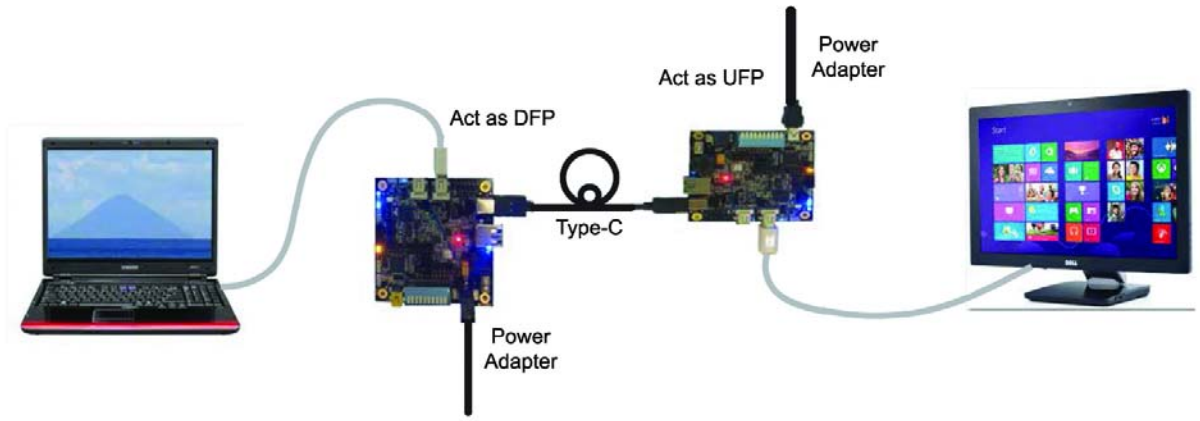
Figure 15. USB Tree Image

```
      ======================== USB Device ========================

       +++++++++++++++++ Device Information +++++++++++++++++
Device Description         : USB Mass Storage Device
Device Path                : \\?\usb#vid_03f0&pid_2340#0176000000027594#{a5dcbf10-6530-11d2-901f-00c04fb951ed}
Device ID                  : USB\VID_03F0&PID_2340\0176000000027594
Driver KeyName             : {36fc9e60-c465-11cf-8056-444553540000}\0056 (GUID_DEVCLASS_USB)
Driver                     : C:\Windows\system32\DRIVERS\USBSTOR.SYS (Version: 6.1.7601.17577  Date: 2013-07-02)
Driver Inf                 : C:\Windows\inf\usbstor.inf
Legacy BusType             : PNPBus
Class                      : USB
Service                    : USBSTOR
Enumerator                 : USB
Location Info              : Port_#0020.Hub_#0001
Location IDs               : PCIROOT(0)#PCI(1400)#USBROOT(0)#USB(20)
Container ID               : {0f3cdbe4-ccb1-5b75-b899-103c71cec05d}
Manufacturer Info          : Compatible USB storage device
Capabilities               : Removable, UniqueID, RawDeviceOK, SurpriseRemovalOK
Address                    : 20
Problem Code               : 0
Power State                : D0 (supported: D0, D3, wake from D0)
 Child Device 1            : Disk drive
  Device ID                : USBSTOR\DISK&VEN_HP&PROD_X705W&REV_1100\017600000002759 4&0
  Class                    : DiskDrive
   Volume                  : \\?\Volume{6c071703-a7dc-11e4-91ca-f01faf517387}\
   Kernel Name             : \Device\HarddiskVolume15
   Mountpoint              : F:\

       ---------------- Connection Information ----------------
Connection Index           : 0x14
Connection Status          : 0x01 (DeviceConnected)
Current Config Value       : 0x01
Device Address             : 0x1B
Is Hub                     : 0x00 (no)
Number Of Open Pipes       : 0x02 (2)
Device Bus Speed           : 0x03 (SuperSpeed)
Pipe0ScheduleOffset        : 0x00 (0)
Pipe1ScheduleOffset        : 0x00 (0)

       ------------------- Device Descriptor -------------------
bLength                    : 0x12 (18 bytes)
bDescriptorType            : 0x01 (Device Descriptor)
bcdUSB                     : 0x300 (USB Version 3.00)
bDeviceClass               : 0x00 (defined by the interface descriptors)
bDeviceSubClass            : 0x00
bDeviceProtocol            : 0x00
bMaxPacketSize0            : 0x09 (9 bytes)
idVendor                   : 0x03F0 (Hewlett Packard)
idProduct                  : 0x2340
bcdDevice                  : 0x1100
iManufacturer              : 0x01
```

Display Port (DP) Alternate Mode

Figure 16 shows the test setup for DP alternate mode.

Figure 16. Test Setup for DP



To test for DP, you need to use one iCE40LP8K DP source board and one iCE40LP8K DP sink board. Refer to EB99, USB Type-C Demo Kit V2 Board User Guide for source/sink board population option. The DP source board has CN1 populated and connected to super speed lines. The DP sink board has CN3 installed and connected to super speed lines. The source board must be a DFP and the sink board a UFP. You can force the initial roles explicitly either by setting the switches as given in Table 7 or implicitly by powering the source board using a power adapter and sink board using USB mini cable. You can also set the roles dynamically by doing data role swap.

To test DP:

1. Connect mini DP male to male cable from laptop to DP source board's DP connector (CN1).
2. Connect DP male to mini DP male cable from DP display to DP sink board's DP connector (CN3).
3. Connect Type-C cable between the two USB Type-C boards.
4. Probe on R197 HPD Signal pad, which becomes logic high from logic low to indicate sink device is connected.
5. Send display data from the laptop to the display by enabling duplicate/extend functions from the keyboards.

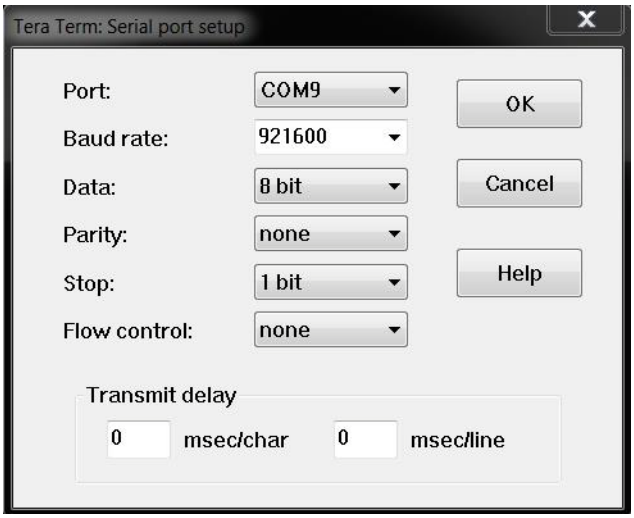
Transaction Logging

Demo 1 supports transaction logging using a terminal application on a computer.

To set up transaction logging:

1. Short jumper J16.3 and J16.2.

Figure 17. Settings in Tera Term

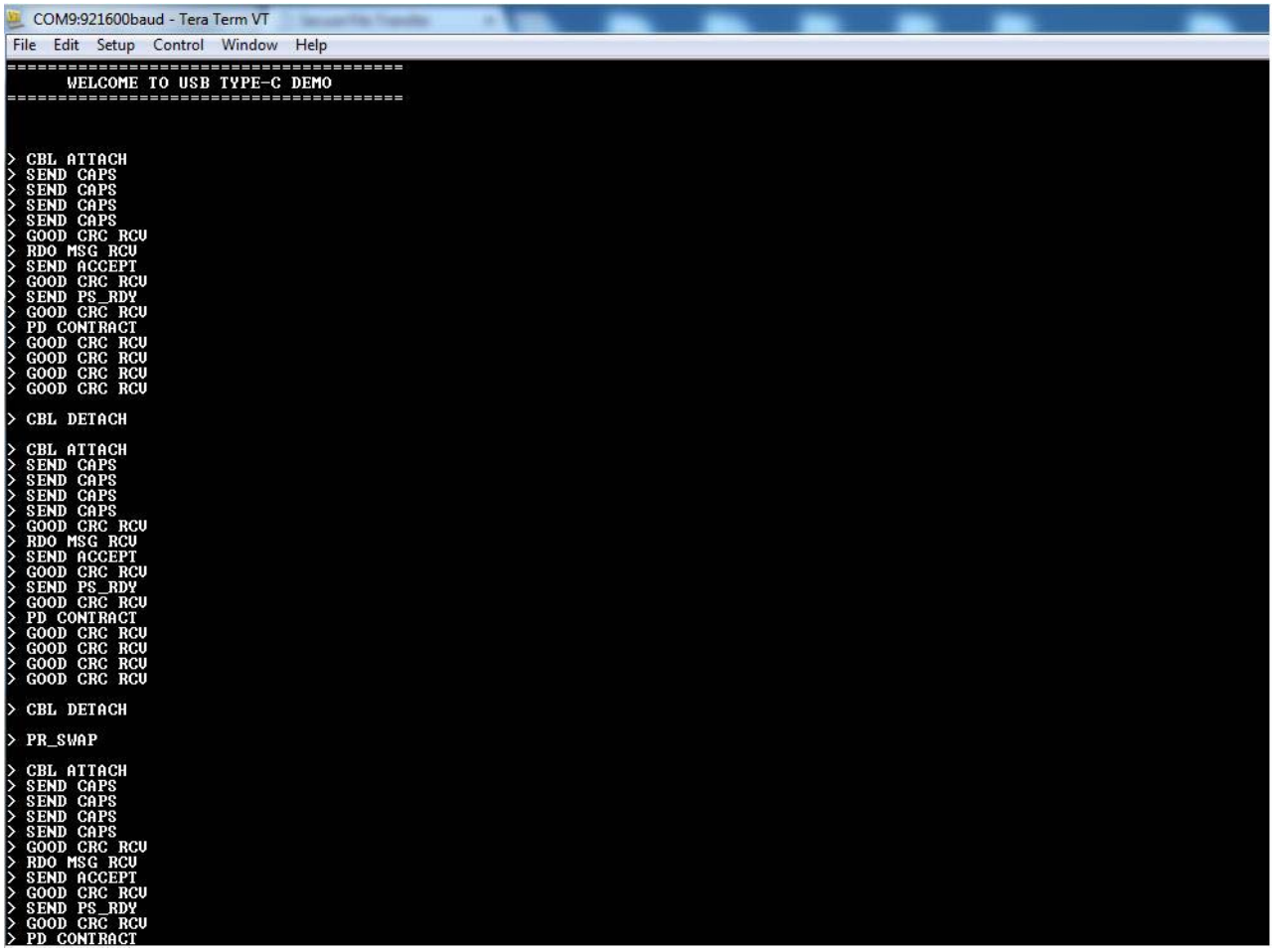


2. Connect any one board to computer using a USB Type-B mini to USB Type-A standard cable.
3. Open hyper-terminal (Tera Term) and apply the settings as shown in Figure 17.
4. Run the demo tests as described previously.

Note: You may need to set the COM port differently from what is shown in Figure 17, depending on the port to which it is connected.

Important events and BMC traffic are displayed in the terminal as they happen. Refer to Figure 18 for data logging status.

Figure 18. Transaction Logging



Demo 2: DRP and Lattice Alternate Mode Demo with iCE40 Device

Demo Board can aggregate two I^2C and eight GPIO signals on board. Aggregator signals can also be driven externally by setting the jumper (J10) which indicates whether aggregated signals are driven externally or internally.

Refer to Table 3, Demo 2 Description for LED status.

To perform test for an aggregator using externally driven signals:

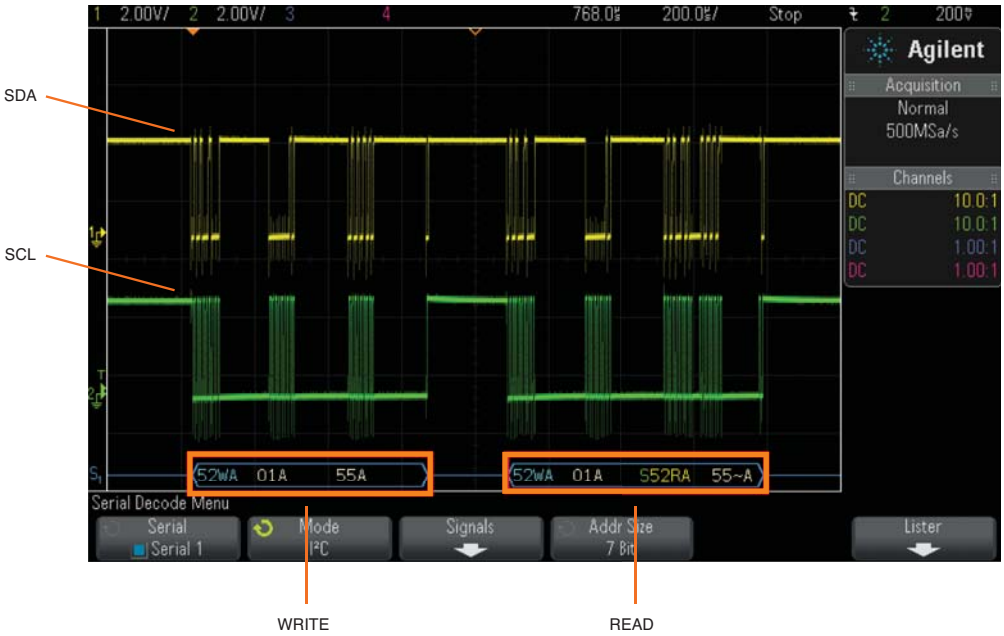
1. Set one board as DFP and other board as UFP. Refer to Table 6 for the settings.
2. Connect J12.1 and J12.2 on one board to configure it as an aggregator output device.
3. Connect J12.2 and J12.3 on another board to configure it as an aggregator input device.
4. Connect J10.2 and J10.3 on both boards to drive an aggregator signals externally.
5. Connect J19.12 (SCL) and J19.14 (SDA) to the external I^2C master lines (in this case, Aardvark I^2C Master), J19.9 (SCL) and J19.11 (SDA) to the external I^2C slave lines (in this case, the Lattice Pico board).
6. Connect the input strobe signals from external device to J19.1, J19.3, J19.5 and J19.7 on the board which acts as an aggregator output device.
7. Connect the input strobe signals from external device to J19.4, J19.6, J19.8 and J19.10 on the board which acts as an aggregator output device. The output strobe signals can be taken to external device from headers J19.1, J19.3, J19.5 and J19.7 on other board which acts as an aggregator input device.
8. On the board acting as DFP, set the DP switch SW3.10 Down to enable the Lattice Alternate mode.
9. Connect two Demo Boards using Type-C cable. LED D24 glows indicating an aggregator enabled on the boards and entered to Lattice alternate mode. Perform I^2C and Strobe transactions and observe the aggregated signals through LEDs.

To perform test for an aggregator driven internally:

1. Set one board as DFP and other board as UFP. Refer to Table 6 for the settings.
2. Connect J12.1 and J12.2 on the DFP board to configure it as an aggregator output device.
3. Connect J12.2 and J12.3 on the UFP board to configure it as an aggregator input device.
4. Connect J10.1 and J10.2 on both boards to drive an aggregator signals from internal device (XO2).
5. On the board acting as DFP, set the DP switch SW3.10 Down to enable the Lattice Alternate mode.
6. Connect two Demo Boards using a Type-C cable. LED D24 glows indicating an aggregator enabled on the boards and entered to Lattice Alternate mode. LEDs D1-D8 indicates the status of an aggregator signal (transmit and receive). Refer to Table 3 for the status LEDs. LEDs D5-D8 indicate I^2C Data which toggles between ”A” and “5”. LEDs D1-D4 displays the 4-bit binary count value.
7. Probe J19.9 and J19.11 for I^2C an aggregator input data.
8. Probe J19.12 and J19.14 for I^2C an aggregator output data.

Refer to Figure 19 for the waveforms.

Figure 19. Internal Aggregator Input and Output Waveforms



Refer to Table 3, Demo 2 Description column for the descriptions of LEDs while running Lattice Alt Mode-Aggregator demos.

Demo 3: DRP Demo with iCE40 Ultra Device

Demo 3 is performed using boards built with Lattice iCE40 Ultra device. The demo design uses Mico8 to implement some of the higher level layers of the Type-C PD specifications. Only a subset of the tests from Demo 1 are supported for Demo 3 as given below:

- Before Cable Attach
- Cable Detection (Attach and Detach)
- Flip Mode
- BMC and PD Contract
- SS/HS Switch Muxing and Signaling

Refer to Table 3, Demo 3 Description for LED status.

Reading Status Using Lattice I2C Utility

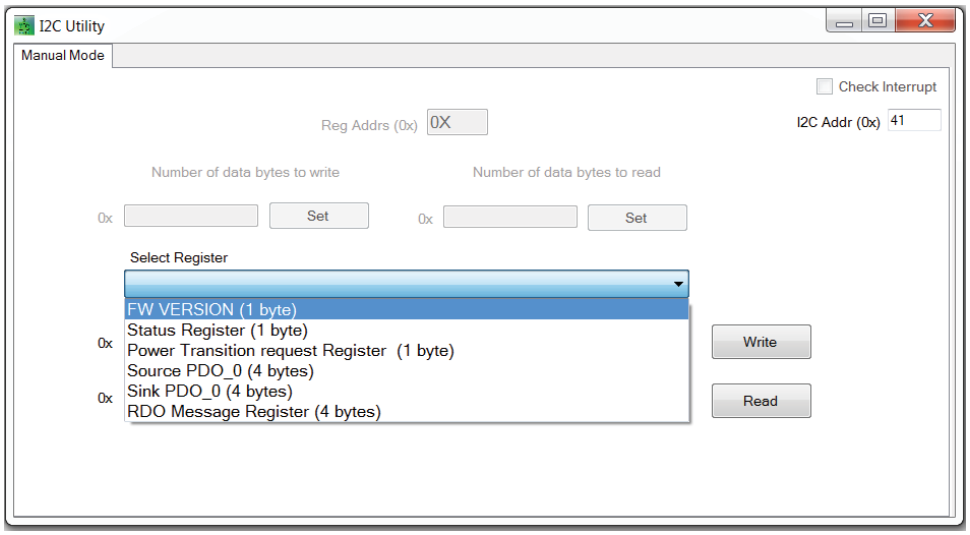
The demo supports reading the device status using Lattice I2C Utility. Before running Lattice I2C Utility, install the supporting software provided in Appendix A. I2C Utility Software Requirements.

To read the status registers:

1. Short jumper J16.2 and J16.3.
2. Connect any one board to computer using a USB Type-B mini to USB Type-A standard cable.
3. Open Lattice I2C Utility and select a register from the drop-down list, as shown in Figure 20.
4. Click **Read** to read the register content. Refer to Appendix B. I2C Read Registers Map Information for register mapping details.

Note: All I2C registers provided are read only registers.

Figure 20. Lattice I2C Utility



Technical Support Assistance

Submit a technical support case via www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
December 2015	1.2	Updated the SW3 switch settings according to USB Type-C Demo Kit V2-Rev B board.
October 2015	1.1	Updated Cable Detection (Attach and Detach) section. Changed LED D21 to LED D20 in step 1 of the procedure for testing cable attach and detach conditions.
		Updated Source Capabilities and Sink Requests section. — Modified Table 6, Supported Source PDOs. Changed 5 V, 3 A Sink PDO to 5 V, 0.9 A. — Modified Table 7, Supported Sink PDOs. Changed 5 V, 3 A Sink PDO to 5 V, 900 mA. — Modified Table 9, Swap Selection. Added Exit VDM Mode in Swap Function.
		Updated Data Role Swap section. Added note.
		Updated Dead Battery section. Added note. Revised dead battery demo procedure.
		Updated SS/HS Switch Muxing and Signaling section. Revised testing HS/SS switch muxing procedure.
June 2015	1.0	Initial release.

Appendix A. I2C Utility Software Requirements

The following software are required to run the I2C Utility:

- **I2C Utility**
  Download the I2C utility from http://www.latticesemi.com/usbcv2.
- **FTDI Drivers**
  Install Lattice Diamond Programmer, which installs FTDI drivers required by the utility, from http://www.latticesemi.com/Products/DesignSoftwareAndIP/ProgrammingAndConfigurationSw/Programmer.aspx.
- **Visual C++ Redistributable Packages for Visual Studio 2013**
  Download the packages from http://www.microsoft.com/en-us/download/details.aspx?id=40784.

Appendix B. I2C Read Registers Map Information

Note: I2C Slave Address 8'h41

- **FW Version** (1 byte)
  Address: x0E
  Data: This register contains the revision number (i.e. xEC)

- **Status Register** (1 byte)
  Address: x02
  Data:

Bit 7	PROLE 0 – Sink 1 – Source)
Bit 6	DROLE 0 – UFP 1 – DFP)
Bit 5	PD Contract 0 – No valid PD contract 1 – Valid PD contract
Bit 4, 0	Reserved

- **Power Transition Request Register** (1 byte)
  Address: x08
  Data: Negotiated PDO number is saved.
- **Source PDO_0** (4 bytes)
  Address: x10
  Data: When current role is PD Source, holds the Source vSafe5V Fixed Supply object.
- **Sink PDO_0** (4 bytes)
  Address: x17
  Data: When current role is PD Sink, holds the Sink vSafe5V Fixed Supply object.
- **RDO Message Register** (4 bytes)
  Address: x2E
  Data: When current role is PD Source, the request packet received for a source capabilities message will be stored here.