2:1 MIPI CSI-2 Image Sensor Aggregator Bridge Demo

User Guide

FPGA-UG-02062 Version 1.2

August 2018

Contents

Figures

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AP	Application Processor
CSI	Camera Serial Interface
DSI	Display Serial Interface
FTDI	Future Technology Devices International
HDMI	High Definition Multimedia Interface
I^2C	Inter-Integrated Circuit
LVDS	Low-Voltage Differential Signaling
SPI	Serial Peripheral Interface
USB	Universal Serial Bus

1. Introduction

This document describes the design and setup procedure for the Lattice Semiconductor 2:1 MIPI® CSI-2 Image Sensor Aggregator Bridge development kit to demonstrate the capabilities of the CrossLink™ FPGA in video applications.

CrossLink 2:1 MIPI CSI-2 aggregator bridge development kit is a set of boards that receives MIPI CSI-2 serial data from two image sensors, combines the image from two cameras and then transmits the combined image data to Application Processor (AP) in MIPI CSI-2 format.

The CrossLink device can receive MIPI DSI/CSI-2 data at the rate of 1.2 Gb/s/lane and transmit it at a rate of 1.5 Gb/s/lane. The device comes with fully validated Soft IPs with flexible controlling options. This demonstration uses the 2:1 MIPI CSI-2 Aggregator Bridge Soft IP.

The development kit consists of three types of boards:

- CrossLink Master Link board featuring a Lattice LIF-MD6000 device
- Raspberry Pi Camera Link boards to connect the Raspberry Pi cameras
- Raspberry Pi AP Link board to connect to Raspberry Pi Model B+ board

Other boards required for the demo apart from the development kit:

- Two Raspberry Pi cameras
- Raspberry Pi Model B+ board to process the MIPI CSI-2 data and display on an HDMI monitor

Figure 1.1 shows the 2:1 MIPI CSI-2 aggregator bridge system diagram.

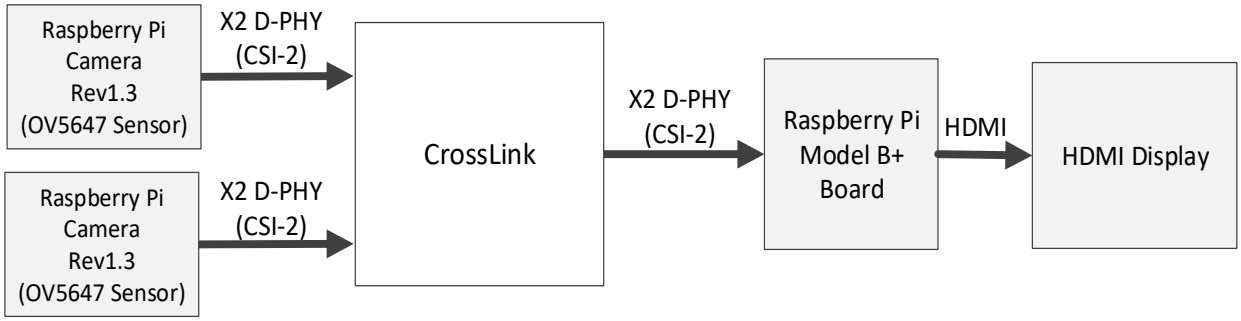


Figure 1.1. 2:1 MIPI CSI-2 Aggregator Bridge System Diagram

2. Functional Description

Figure 2.1 shows the 2:1 MIPI CSI-2 Aggregator IP internal block diagram. The 2:1 MIPI CSI-2 Aggregator IP receives the serial, source-synchronous MIPI data from two MIPI CSI-2 cameras through the Soft D-PHY blocks (programmable I/Os configured as MIPI CSI-2 receivers), deserializes the serial data into bytes and extracts the control signal from MIPI data packets. The IP then combines both cameras' parallel data streams and sends it to the MIPI CSI-2 Transmitter block. The MIPI CSI-2 Transmitter block includes a Hard D-PHY block that serializes the data and sends it out in MIPI CSI-2 format.

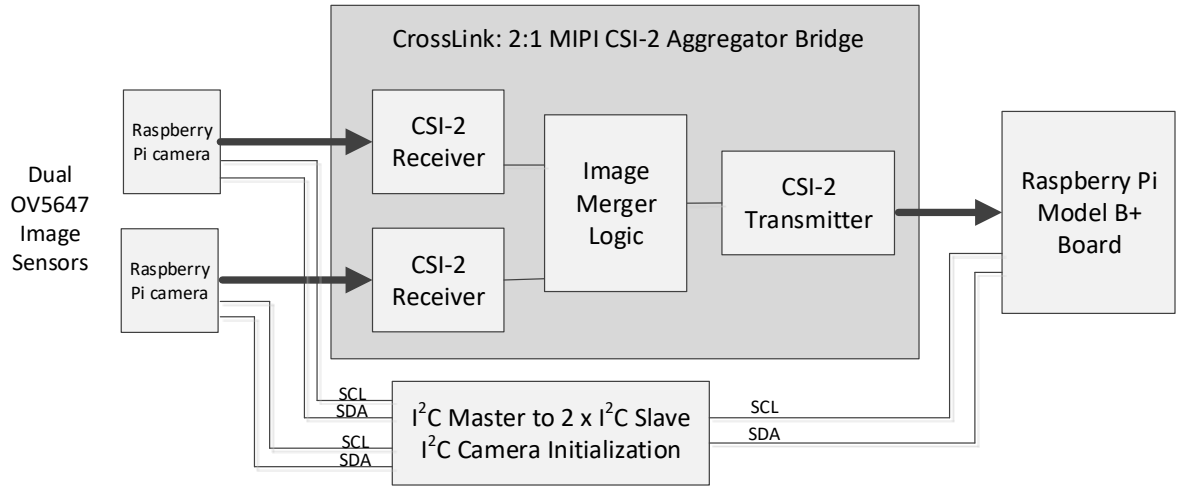


Figure 2.1. Internal Block Diagram of 2:1 MIPI CSI-2 Aggregator Bridge Demo

A single I^2C master to dual I^2C Slave Bridge is used to configure the two Raspberry Pi cameras. The Raspberry Pi Model B+ board is configured as I^2C master and the two Raspberry Pi cameras as slaves. As the Raspberry Pi AP source code is closed, we have implemented special functionalities in MachX03LF to configure the cameras, so that the demo works in such environment. As part of this special functionality, every I^2C command from Raspberry Pi Model B+ board goes to both cameras.

In the MachXO3LF design, the write commands are sent to both cameras simultaneously whereas, the read commands are answered by only one of these cameras. The I^2C design implements the logic in order to change the register settings in the Raspberry Pi camera thus enabling continuous clock mode.

3. Demo Setup

This section describes the demo setup.

3.1. Hardware Requirements

The following equipment are required for the MIPI Dual CSI-2 to CSI-2 demo:

- CrossLink Raspberry Pi 2:1 MIPI CSI-2 Aggregator Demo Kit
  - CrossLink LIF-MD6000 Master Link board
  - Raspberry Pi Camera Link board (2)
  - Raspberry Pi AP link board
- Raspberry Pi 3 Model B V1.2 board or Raspberry Pi Model B+ board.
- Extra FPC cables used for RPi cameras
- Raspberry Pi cameras with FPC cables (2)
- HDMI monitor
- HDMI to HDMI cable
- USB 2.0 Type A to Mini-B cable, included in demo kit
- USB 2.0 Type A to Micro-B cable
- Power adaptors (2), included in demo kit
- Laptop

3.2. Software Requirements

- Lattice Diamond® Programmer version 3.10 or later
- JED File for MachXO3LF
- BIT File for CrossLink

3.3. Board Setup

Figure 3.1 shows the top view of the CrossLink LIF-MD6000 Master Link board used in this demo. Figure 3.2 shows the Raspberry Pi AP Link Board and the Raspberry Pi Camera Link Board. For more details about these boards, refer to www.latticesemi.com/masterlink.

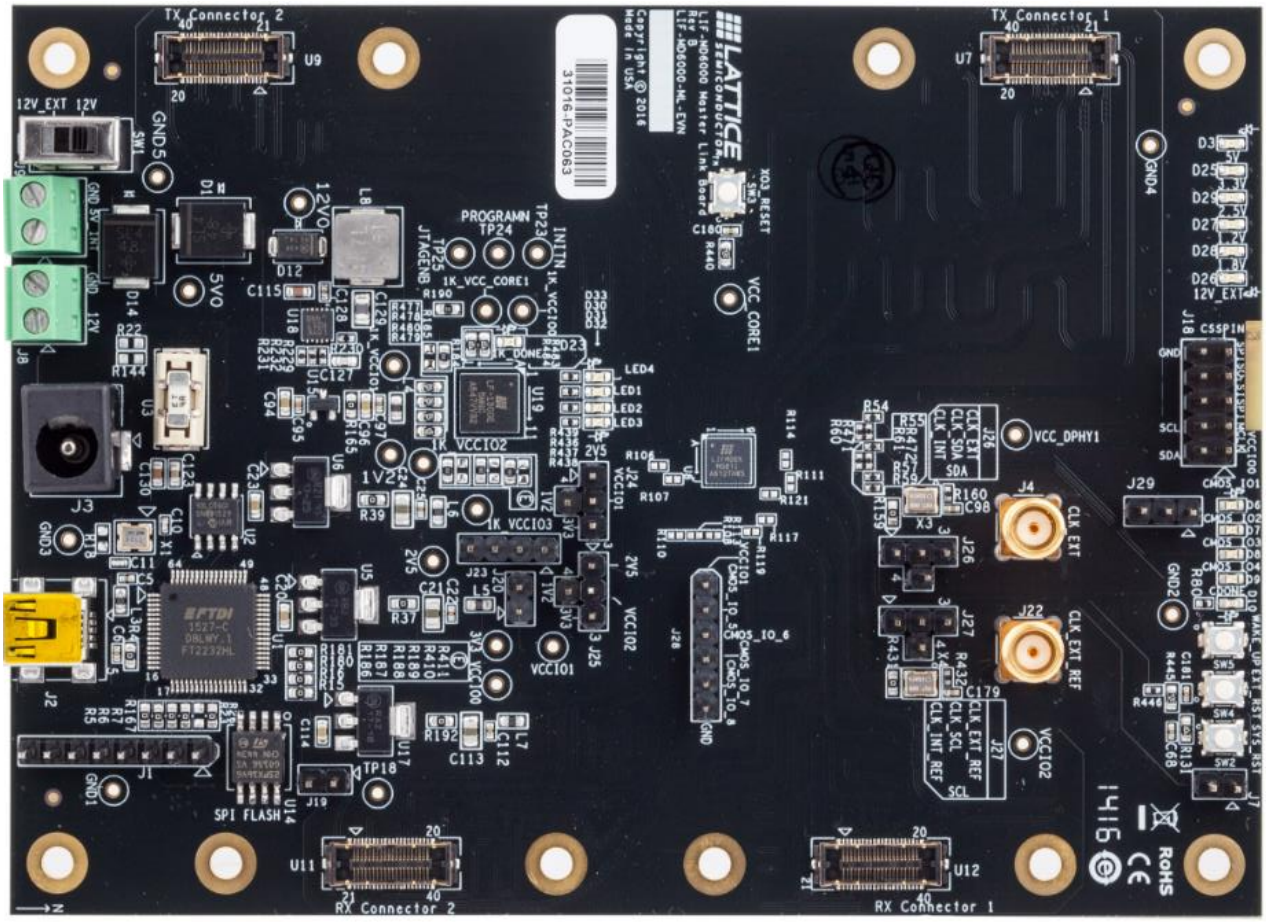


Figure 3.1. CrossLink LIF-MD6000 Master Link Board

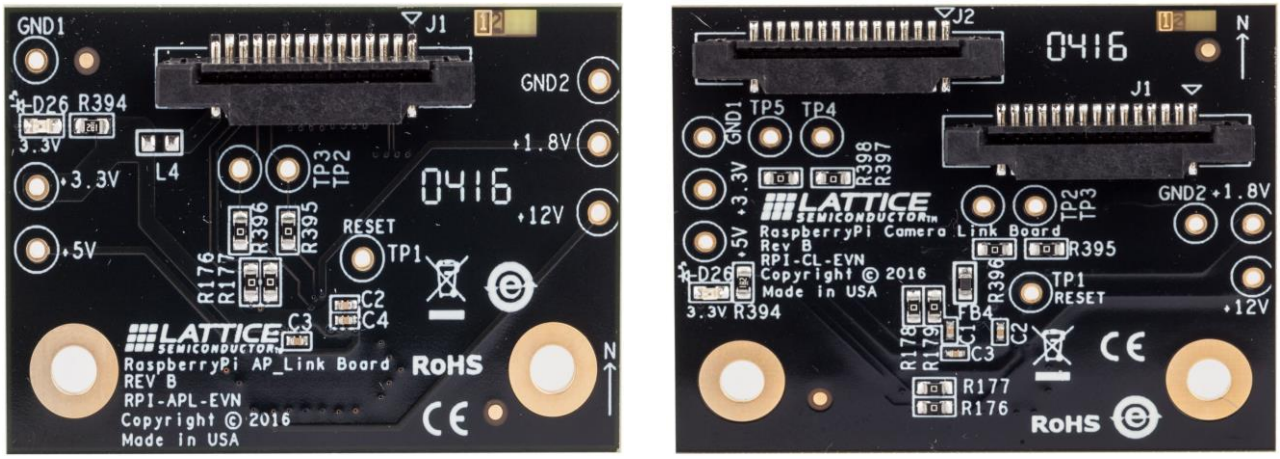


Figure 3.2. Raspberry Pi AP Link Board and Raspberry Pi Camera Link Board

Note: This demo requires two Raspberry Pi cameras (referred in the procedure as camera 1 and camera 2). These cameras share a single oscillator in order to synchronize them.

To set up the hardware for the 2:1 MIPI CSI-2 aggregator demo:

1. Follow the rework procedure below based on the version of the camera module. Attach the two boards to each other to ensure that the rework stays securely in place.

   For Camera Module v1.3 using the OmniVision sensor, follow the steps below.

   a. Remove the Y1 oscillator from the camera 1 board.
   b. Take the camera 2 board and connect the test point beside the oscillator of the camera 2 board to the same test point on the camera 1 board.
   c. Connect a wire to a GND point on the camera 1 board and connect it to a GND point on camera 2 board.

      Note that Figure 3.3 does not show the GND wire connection.

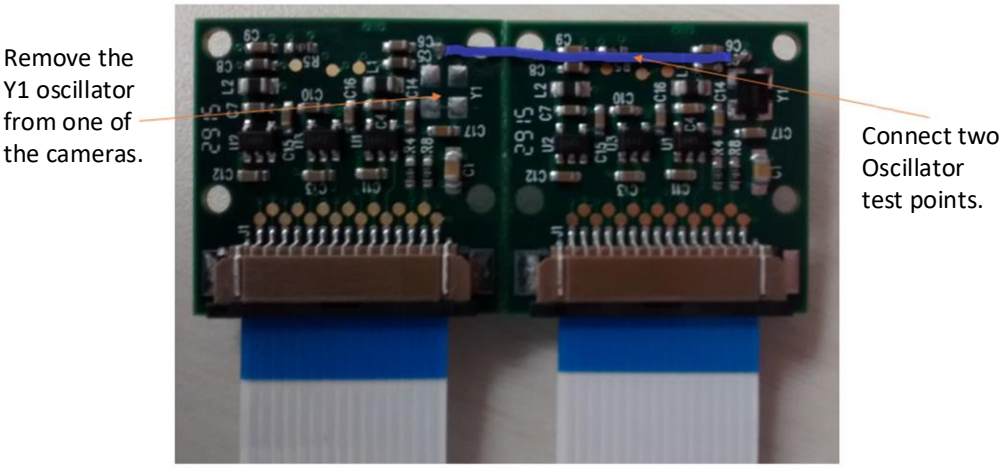


Figure 3.3. Rework of Raspberry Pi Cameras v1.3.

   For Camera Module v2.1 using the Sony sensor, follow the steps below.

   a. Remove the X1 oscillator from the camera 1 board.
   b. Place a wire between R3 (on the side that is connected to X1.3 of the oscillator) of the two boards.
   c. Connect a wire between GND points on each board, such as on C9 GND side (the pad that is closest to the edge of the PCB).

2. Connect the U1 connector of the two Raspberry Pi Camera Link boards to the Rx connector1 and the Rx connector2 of CrossLink Master Link board respectively.
3. Connect the U1 connector of the Raspberry Pi AP Link Board to the TX connector1 of the LIF-MD6000 Master Link board.
4. Fix all the boards tightly with bolts and spacers as shown in Figure 3.4.
5. Populate jumpers J20, J19, J7 and J29 (2-3).
6. Connect the jumpers between pin2 and pin4 on both J24 and J25.
7. Connect the Raspberry Pi cameras with the FPC cables to the J1 connector on the two Raspberry Pi Camera Link boards.
8. Connect one end of the extra FPC cable to J1 of AP Link Board and the other end to the J3 camera connector on the Raspberry Pi Model B+ board.
9. Connect the HDMI port of the Raspberry Pi Model B+ board to a monitor via HDMI cable. See Figure 6.1.
10. Connect a keyboard to one of the USB Type-A ports on the Raspberry Pi board.

11. Connect a mouse to the other USB Type-A port on the Raspberry Pi board.
12. Connect the Raspberry Pi board using the USB-micro power adapter. This powers-up the Raspberry Pi board.
13. Wait for the desktop environment to initialize.

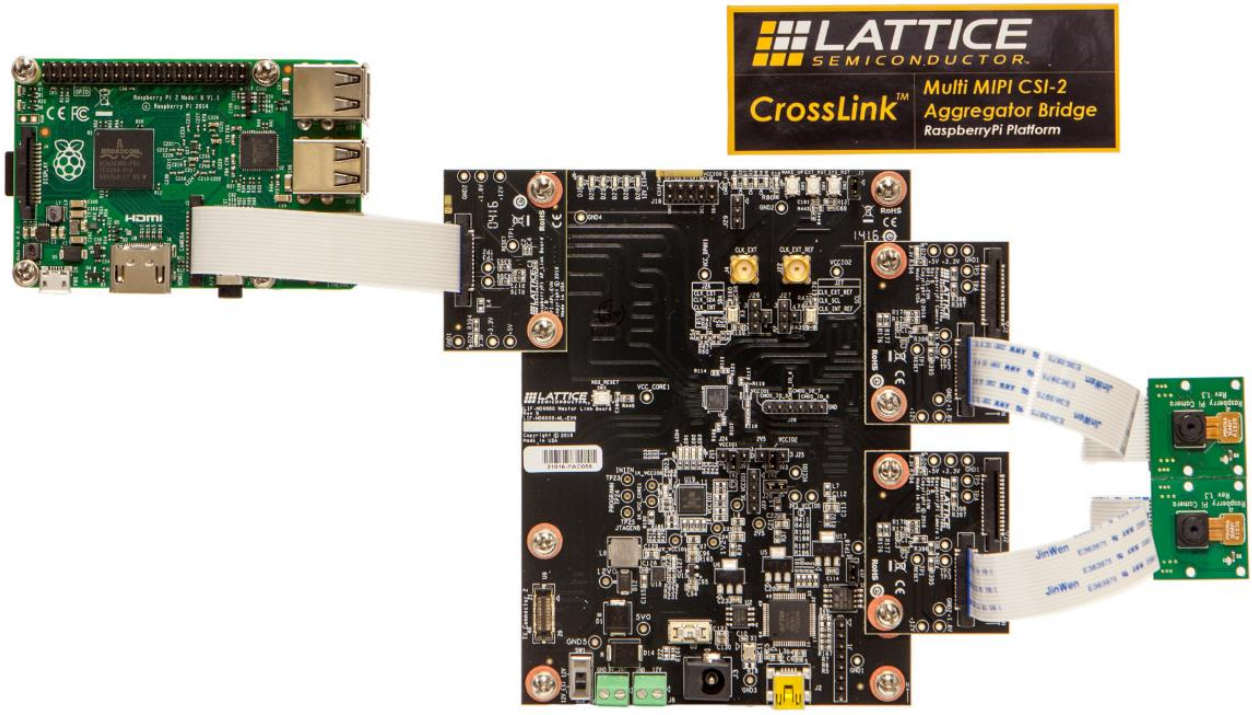


Figure 3.4. Assembled Demo System

4. Programming and Configuration

This section explains the programming and configuration settings of the 2:1 MIPI CSI-2 aggregator demo kit.

The 2:1 MIPI CSI-2 Aggregator demo kit supports the programming of FPGA devices from flash device or directly through FTDI chip using Mini USB (J2) connector. The programming mode and device selection is done in Lattice Diamond Programmer. All design files required for running this demo are available on Lattice website.

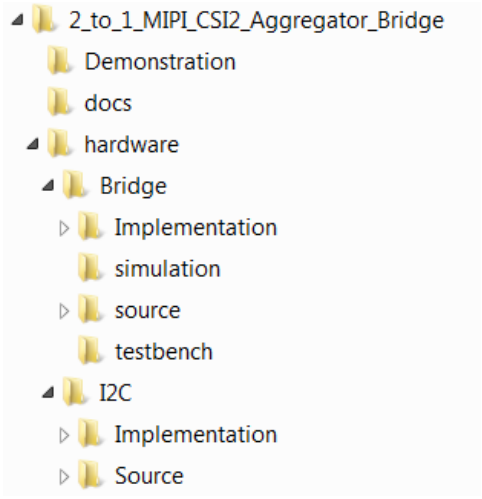


Figure 4.1. 2:1 MIPI CSI-2 Aggregator Bridge Demo Package Directory Structure

The **Demonstration** folder includes the bit file and JED file required for programming the CrossLink LIF-MD6000 device and the Lattice MachXO3LF device, respectively.

The packaged design contains two Lattice Diamond projects within the ***Hardware\Bridge\implementation*** folder. These projects are configured for CrossLink and MachXO3LF devices for the Aggregator Bridge and the I^2C designs respectively.

4.1. Clarity Designer Settings

To configure the demo in Clarity Designer:

1. Install Lattice Diamond 3.10.
2. Open Clarity Designer.
3. Download and install the **csi2_to_csi2** IP.
4. View the IP in the IP catalog as shown in Figure 4.2.

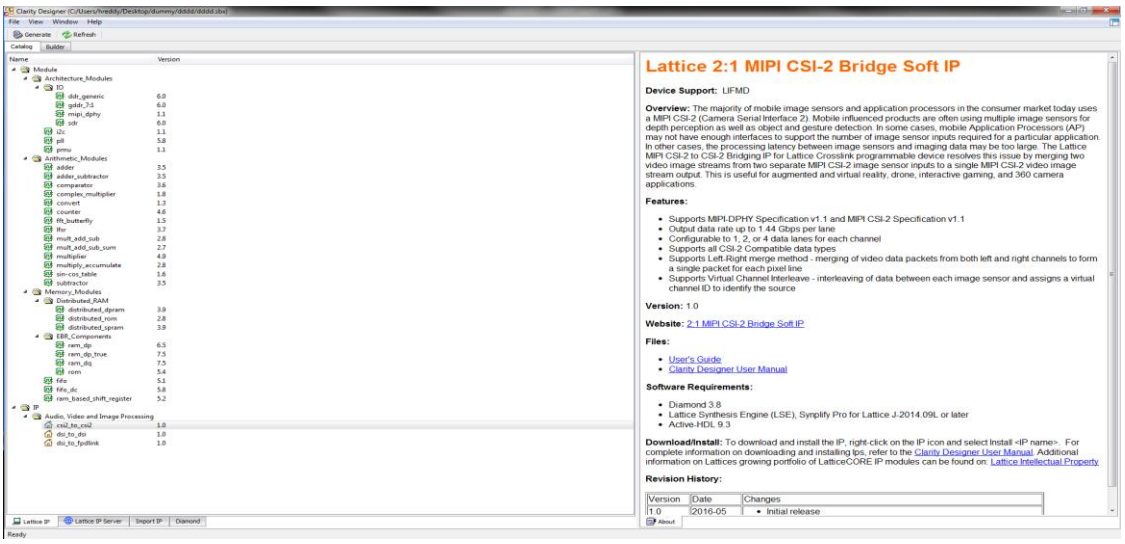


Figure 4.2. csi2_to_csi2 IP in IP Catalog

5. Use the settings shown in Figure 4.3 and Figure 4.4 to configure the IP for running this demo. The project already comes with these settings set in the IP.

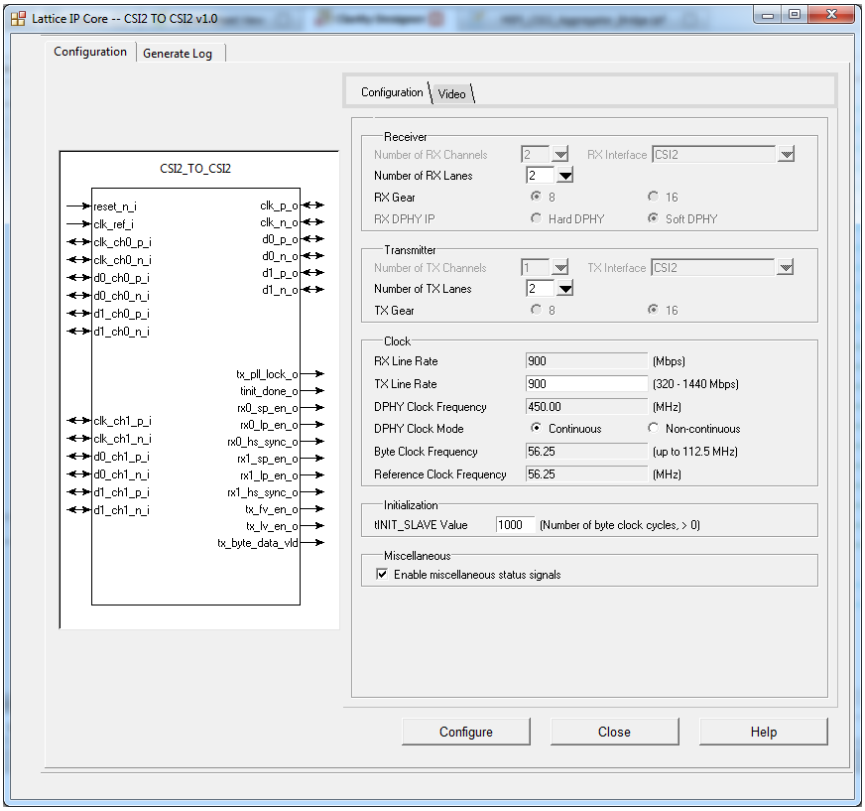


Figure 4.3. Configuration Settings for csi2_to_csi2 IP

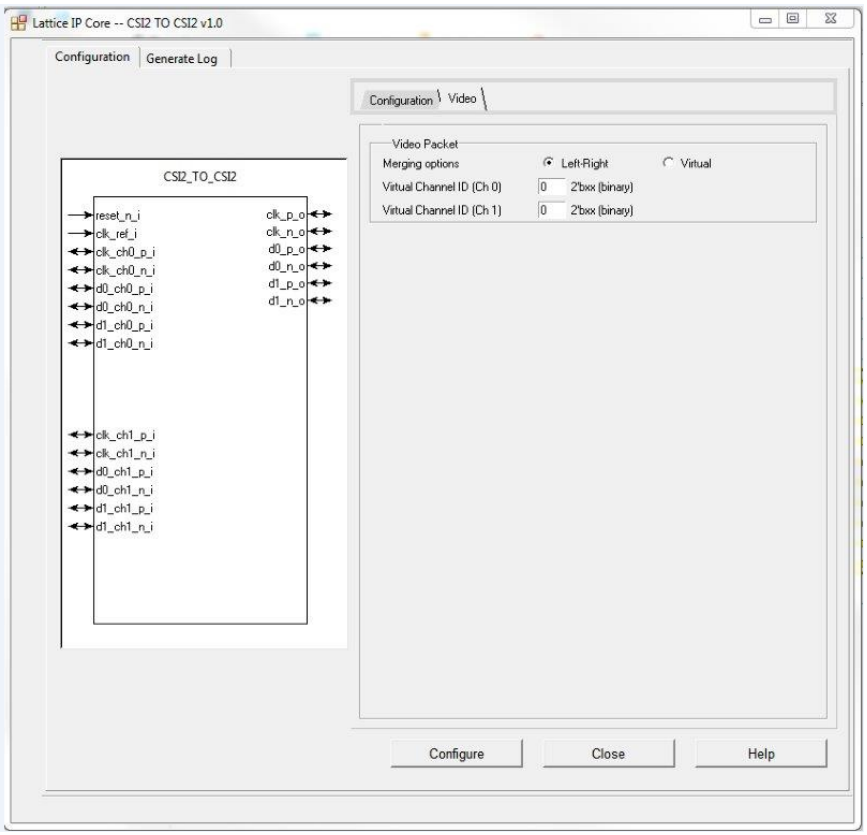


Figure 4.4. Other Settings for csi2_to_csi2 IP

6. Generate the design.
7. Go to the Clarity Designer generated **<instance_name>.lpc** file and change the following parameters:
   - videomerge=HALF_MERGE
   - txgear=8

4.2. Pinout

The pinout shown in Figure 4.5 is used for this demo design to run with the Raspberry Pi hardware. In the original design, the **csi2_reset_n_i** signal is placed on ball G9 of the CrossLink device. Ball G9 is located in bank 2 which is set to 1.2 V since some of the signals in this bank are configured as MIPI D-PHY CSI-2 inputs. However, LVCMOS12 inputs are no longer supported in Crosslink. Diamond 3.8 and later versions no longer allows this signal to be placed on ball G9. Signal **csi2_reset_n_i** can be moved to a ball in bank 0, which is configured for 3.3 V, as a workaround.

In addition to assigning the signal to bank 0, some re-work to the Master Link Board is required. For example, if **csi2_reset_n_i** is assigned to J2, the following rework is needed. R446 and R415, both 0 Ω resistors, should be removed. A wire needs to be added to connect the switch side of R446 pad and the J2 ball side of the R415 pad.

Pinout by Port Name:

Port Name	Pin/Bank	Buffer Type	Site	BC Enable	Properties
csi2_clk_ch0_n_i	G6/1	MIPI_IN	PB29B		DRIVE:2mA CLAMP:ON HYSTERESIS:ON
csi2_clk_ch0_p_i	G7/1	MIPI_IN	PB29A		DRIVE:2mA CLAMP:ON HYSTERESIS:ON
csi2_clk_ch1_n_i	D8/2	MIPI_IN	PB16B		DRIVE:2mA CLAMP:ON HYSTERESIS:ON
csi2_clk_ch1_p_i	D9/2	MIPI_IN	PB16A		DRIVE:2mA CLAMP:ON HYSTERESIS:ON
csi2_clk_n_o	A9/60	DPHY_BIDI	DPHY0_CKN		
csi2_clk_p_o	A8/60	DPHY_BIDI	DPHY0_CKP		
csi2_d0_ch0_n_i	E2/1	MIPI_IN	PB38B		DRIVE:2mA CLAMP:ON HYSTERESIS:ON
csi2_d0_ch0_p_i	E1/1	MIPI_IN	PB38A		DRIVE:2mA CLAMP:ON HYSTERESIS:ON
csi2_d0_ch1_n_i	F8/2	MIPI_IN	PB2B		DRIVE:2mA CLAMP:ON HYSTERESIS:ON
csi2_d0_ch1_p_i	F9/2	MIPI_IN	PB2A		DRIVE:2mA CLAMP:ON HYSTERESIS:ON
csi2_d0_n_o	A7/60	DPHY_BIDI	DPHY0_DN0		
csi2_d0_p_o	B7/60	DPHY_BIDI	DPHY0_DP0		
csi2_d1_ch0_n_i	D2/1	MIPI_IN	PB34B		DRIVE:2mA CLAMP:ON HYSTERESIS:ON
csi2_d1_ch0_p_i	D1/1	MIPI_IN	PB34A		DRIVE:2mA CLAMP:ON HYSTERESIS:ON
csi2_d1_ch1_n_i	H8/2	MIPI_IN	PB6D		DRIVE:2mA CLAMP:ON HYSTERESIS:ON
csi2_d1_ch1_p_i	H9/2	MIPI_IN	PB6C		DRIVE:2mA CLAMP:ON HYSTERESIS:ON
csi2_d1_n_o	B9/60	DPHY_BIDI	DPHY0_DN1		
csi2_d1_p_o	B8/60	DPHY_BIDI	DPHY0_DP1		
csi2_reset_n_i	G9/2	LVCMOS12_IN	PB2C		PULL:UP CLAMP:ON HYSTERESIS:ON

Figure 4.5. Pinout

4.3. I²C Design

Below is the block diagram for the I²C design that is used in the MachXO3LF device. It takes the I²C commands from Raspberry Pi AP board and use it to configure both Raspberry Pi cameras.

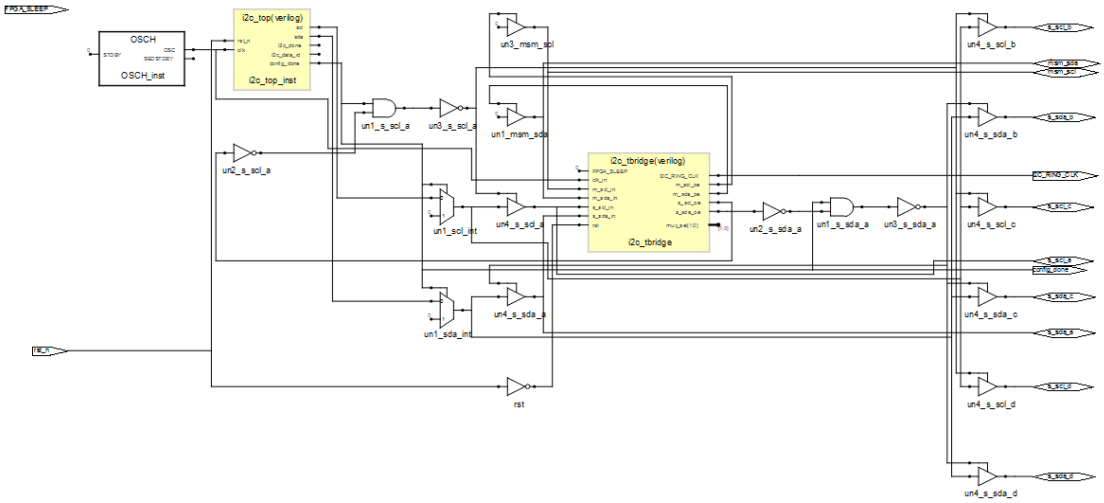


Figure 4.6. Block Diagram of I²C Design

The i2c_top module is used for configuring the cameras directly with the commands from the FPGA. It has an initialization ROM which you can use for storing the camera initialization commands and for configuring the cameras. Once the camera initialization is completed, the config_done signal goes high. Since the cameras are not configured from the FPGA in this demo, the config_done signal is tied to high. Once the config_done signal is high, SCL and SDA lines are given control to the i2c_tbridge module. Figure 4.7 shows the internal block diagram of the i2c_tbridge.

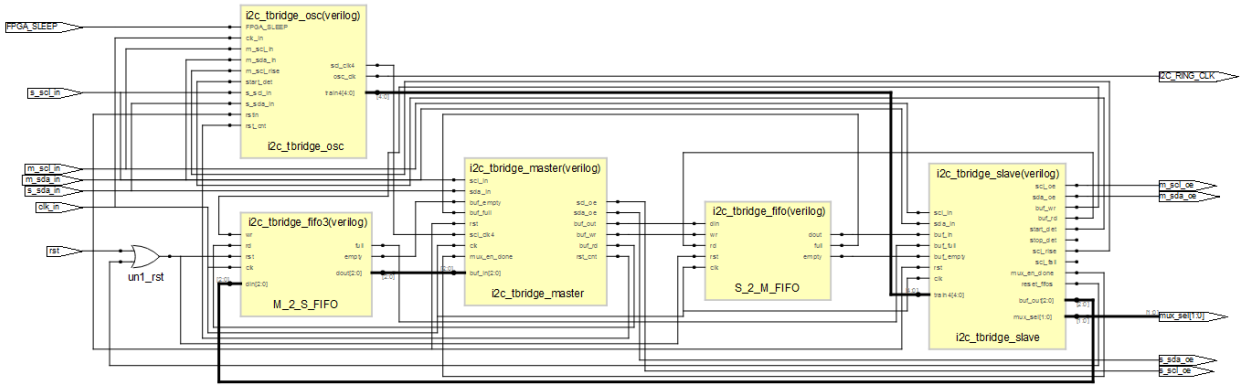


Figure 4.7 i2c_tbridge Module Internal Block Diagram

The i2c_tbridge_slave module receives the I^{2}C commands from an external I^{2}C master (Raspberry Pi AP) and then stores these commands to i2c_tbridge_fifo3. The i2c_tbridge_master reads these commands from the i2c_tbridge_fifo3 and then sends it to the external slaves (Raspberry Pi cameras). During the read back from the cameras, the data is read by i2c_tbridge_master and stored in i2c_tbridge_fifo which are sent back to the external master by i2c_tbridge_slave. During the read back from the cameras, only data from one camera is considered.

4.4. Programming the Board

To program the board:

1. Connect the Mini USB cable to the LIF-MD6000 Master Link Board.
2. Open the Lattice Diamond Programmer tool version 3.10 or later. The window shown in Figure 4.8 appears.
3. Click **OK**.

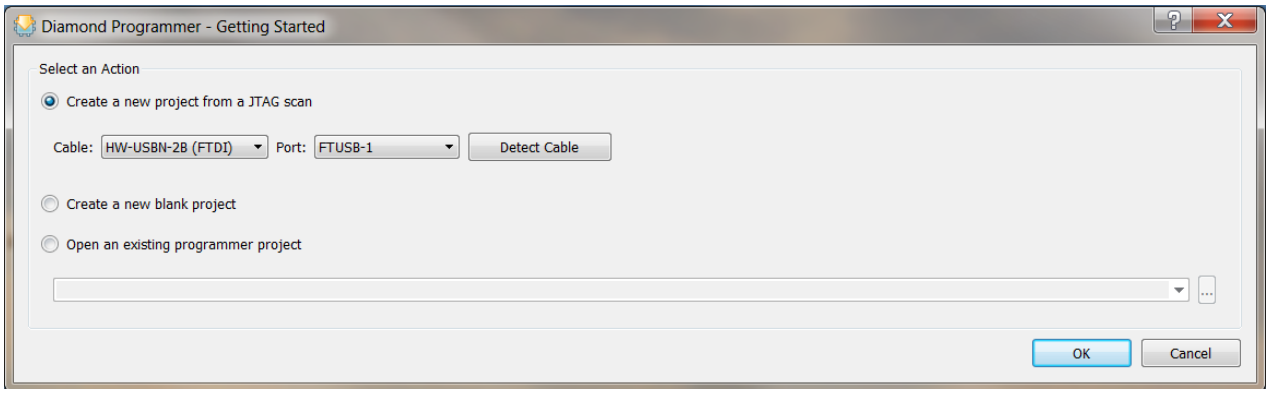


Figure 4.8. Diamond Programmer – Getting Started

4. The Diamond Programmer automatically scans the device on the board, and the window shown in Figure 4.9 appears.

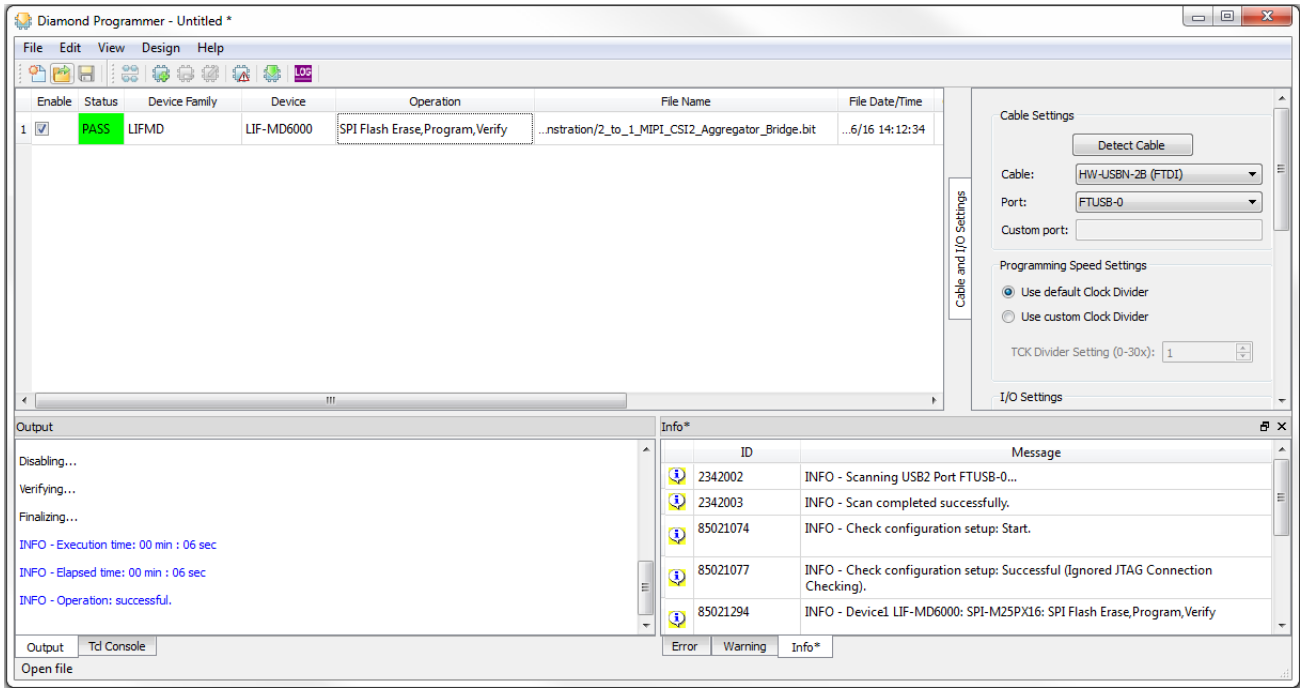


Figure 4.9. Diamond Programmer Main Interface

5. Enable only LIF-MD6000 device and change the operation to SPI Flash Programming.
6. Select the options for the External SPI Flash on the board as shown in Figure 4.10.

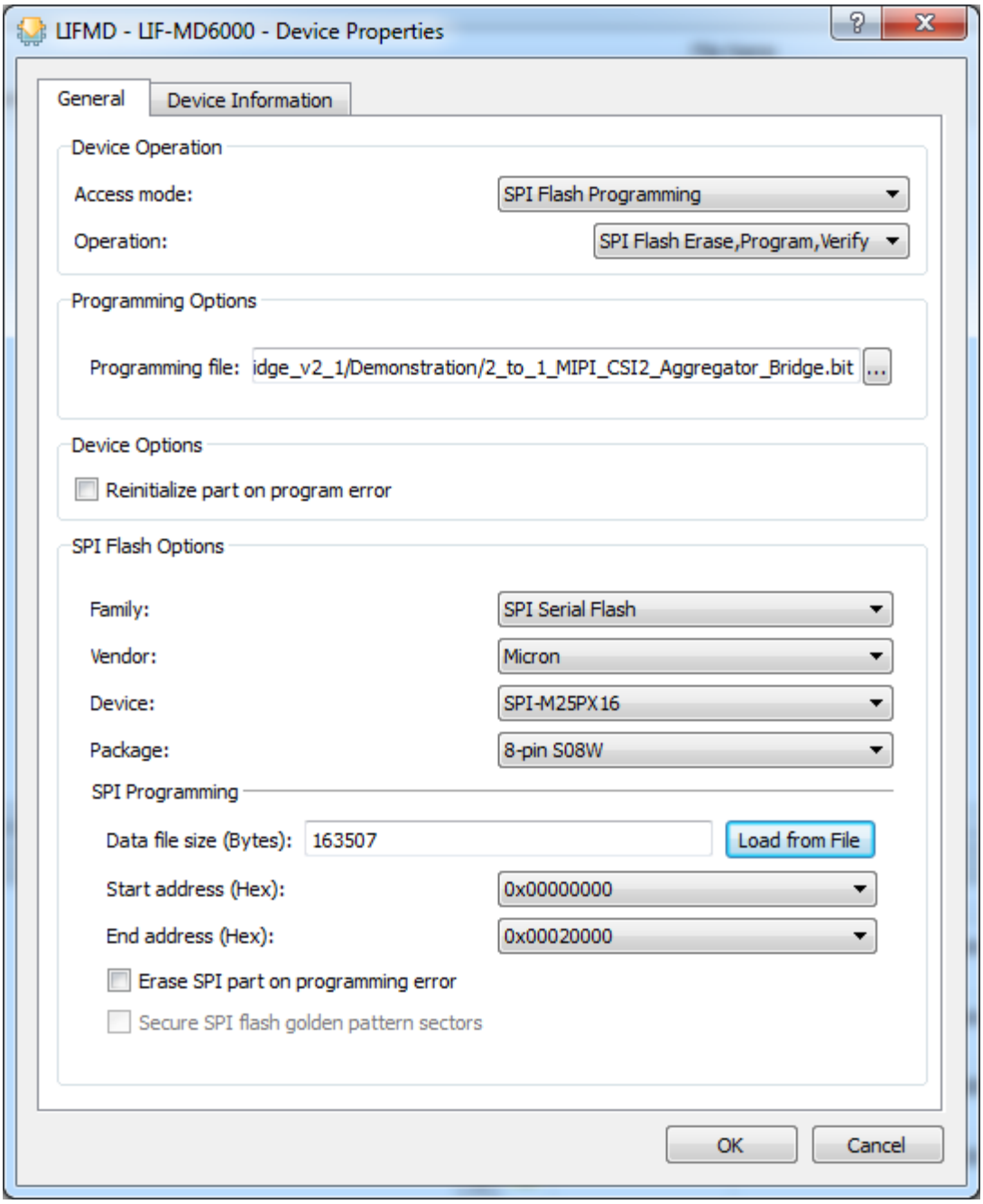


Figure 4.10. LIF-MD6000 Device Properties

7. Provide the location of the bit file **2_to_1_MIPI_CSI2_Aggregator_Bridge.bit** and click **Load from File**.
8. Click **OK**.
9. Click the **Program** button. When programing is completed, the message *INFO - Operation: successful* appears in the output window.
10. Change the **Port** in **Cable settings** (on the right side of Programmer window) from **FTUSB-0** to **FTUSB-1**.
11. On the menu bar click **Design** and select **JTAG Scan**. The MachXO3LF device on the board is scanned by the programmer.
12. Provide the **MachXO3LF I2C.jed** file location and program the device as shown in Figure 4.11. When programing is completed, the message *INFO - Operation: successful* appears in the output window.

The hardware setup is completed.

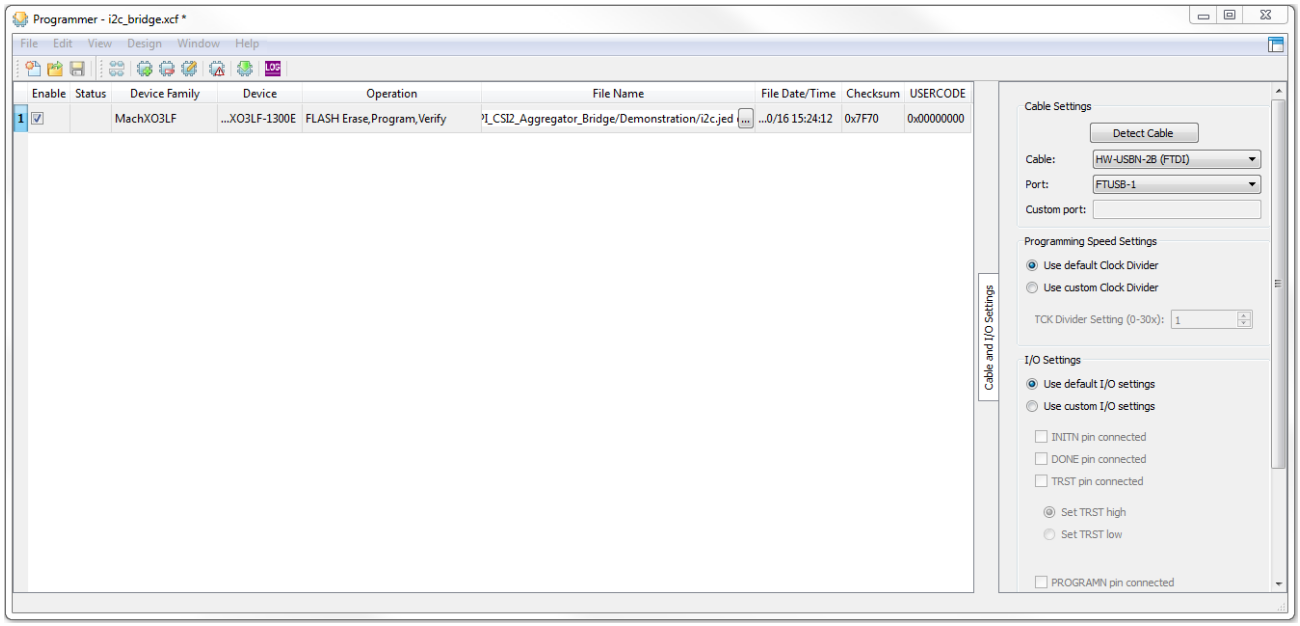


Figure 4.11. MachXO3LF Programming

5. Software Setup

To set up the software for the 2:1 MIPI CSI-2 aggregator bridge demo:

1. Make sure your Raspberry Pi board is updated with the firmware Raspbian Jessie version March 2016 or later. The latest version of the software is available at

   https://www.raspberrypi.org/downloads/raspbian/
2. Open the command prompt.
3. Open the raspi-config tool using command below.

   ```
   sudo raspi-config
   ```
4. Select **Enable camera** and press **Enter**.
5. Go to **Finish** and reboot the computer.

   Note: Perform these steps only once when configuring the setup for the first time.

6. Running the Demo

To run the demo:

1. Run the command below.

   ```
   raspivid -o video.h264 -t 10000
   ```

   The image is displayed. If the message *Waiting for data* appears in the terminal window, press the reset button SW4 on the board. If the image is not displayed after ~5 seconds, press **Ctrl+C** to cancel the raspivid program. Then press SW4 on the Master Link board and repeat the above command.

   The final image from the two cameras appear side by side as shown in Figure 6.1.

2. Press **Ctrl+C** to exit the demo.

Note: Appendix A provides tips to diagnose issues with the 2:1 MIPI CSI-2 aggregator bridge demo. See Appendix A also for details on hardware part numbers and debugging.

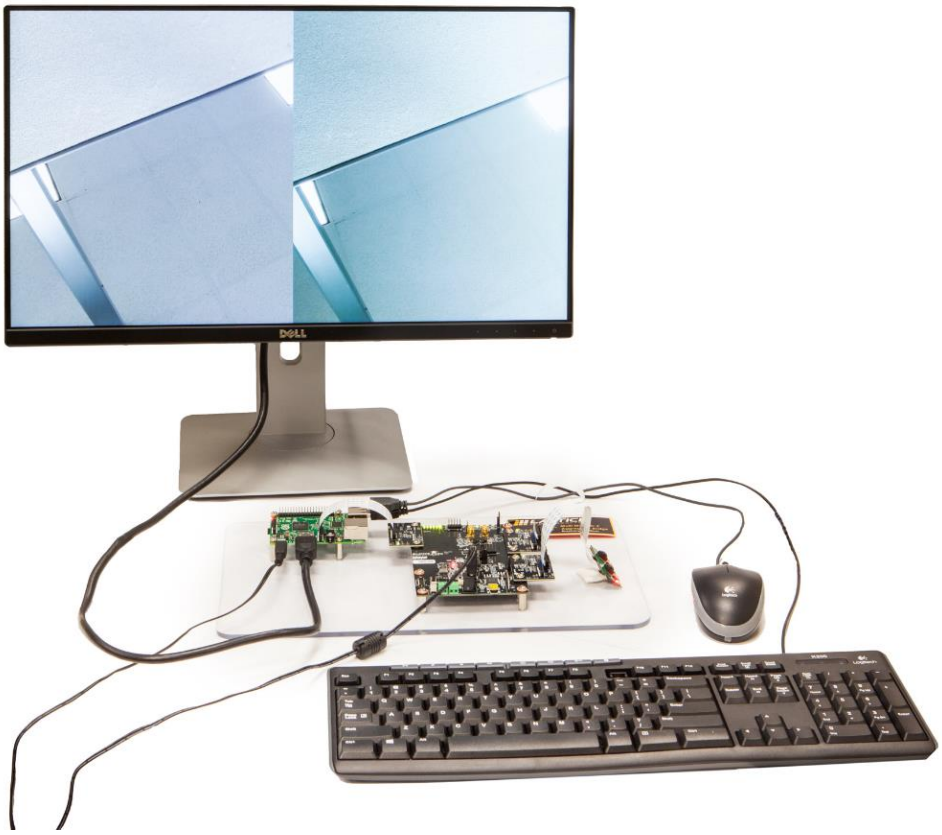


Figure 6.1. Full Setup Showing the Final Output of Demo

7. Ordering Information

Description	Ordering Part Number	Change Summary
Lattice CrossLink Master Link Board	CrossLink-ML-EVN	Initial Release
RPi Camera Link Board	RPI-CL-EVN	Initial Release
RPi AP Link Board	RPI-APL-EVN	Initial Release

Supplemental Information

Additional resources related to the Lattice Dual CSI-2 to CSI-2 kit including updated documentation and design project are available at www.latticesemi.com/rpiboards

Technical Support Assistance

Submit a technical support case via www.latticesemi.com/techsupport.

Appendix A. Debugging

If you encounter issues while using this demo, you may check the following:

1. The version of Raspbian Jessie on the Raspberry Pi should be version March 2016 or later.
2. Run the camera demo by directly connecting the Raspberry Pi camera to the Raspberry Pi Model B+ board.
3. Ensure that the cables from the camera to the RPi Camera Link boards are connected properly.
4. Check the jumper settings.
5. When running the command below, GPIO1 (TP2) and GPIO2 (TP3) on the Raspberry Pi AP Link Board should go high.

```
raspivid –o video.h264 –t 10000
```

Appendix B. LIF-MD6000 Master Link Board Schematics

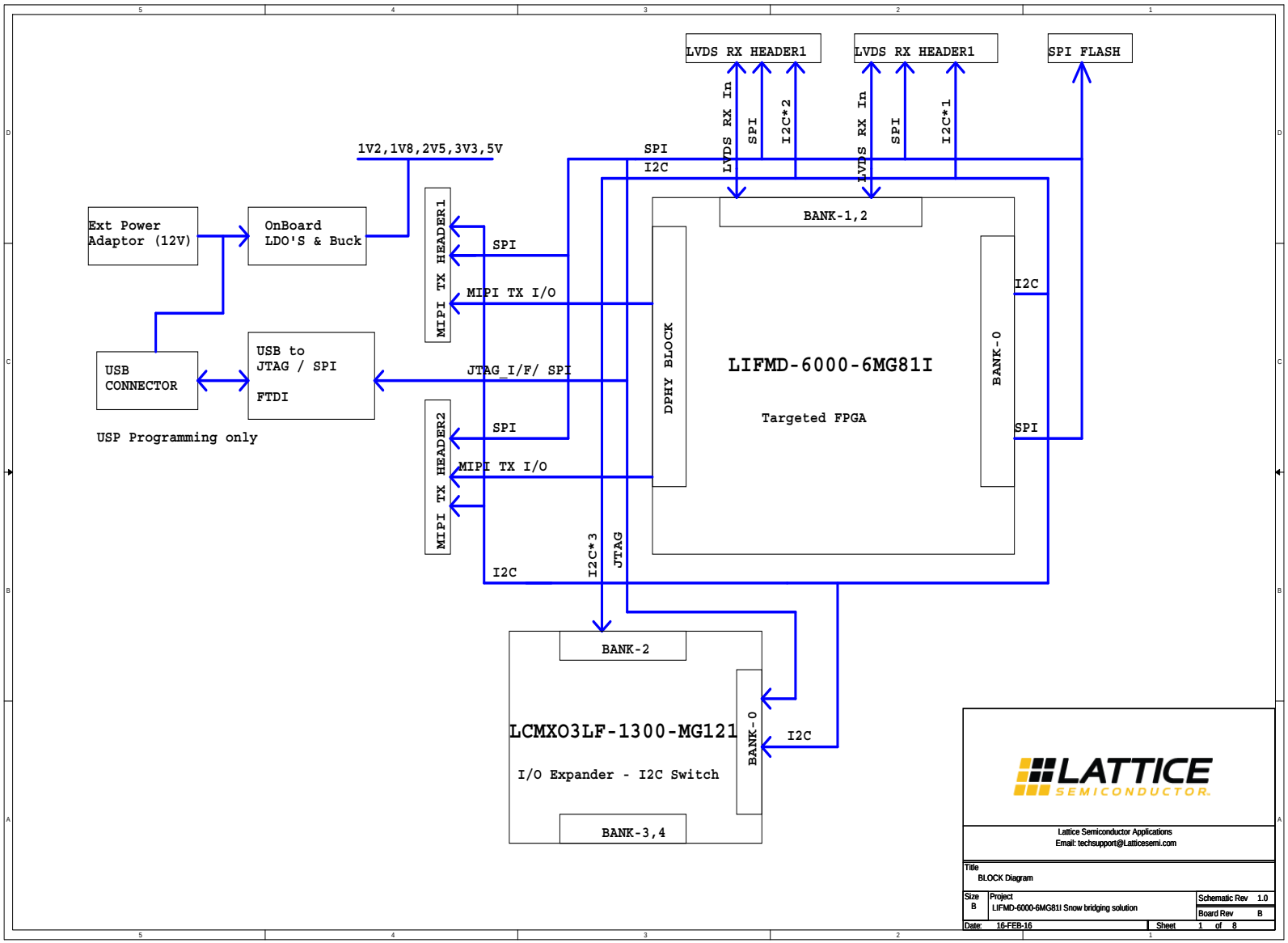


Figure B.1. Block Diagram

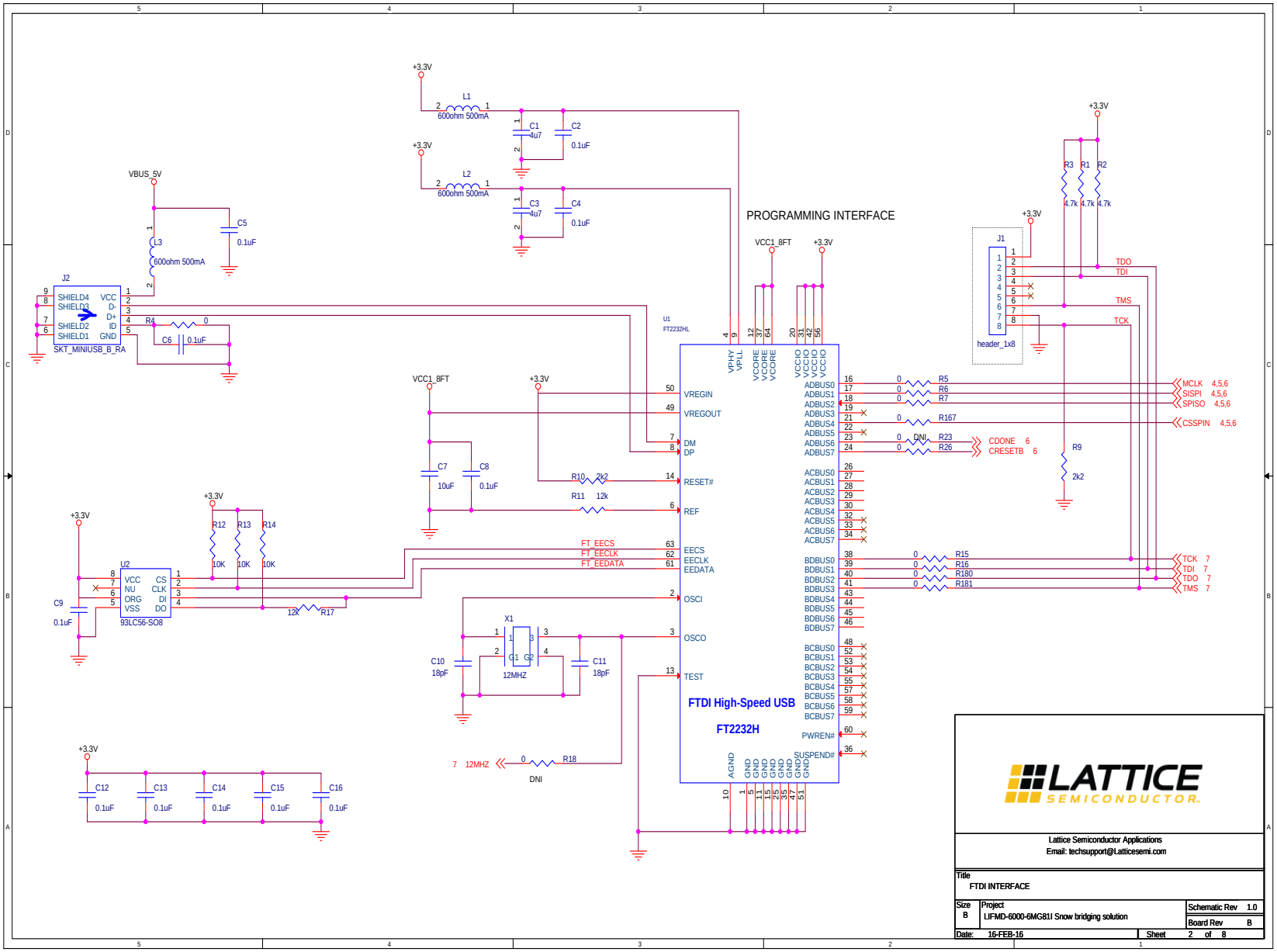


Figure B.2. FTDI Interface

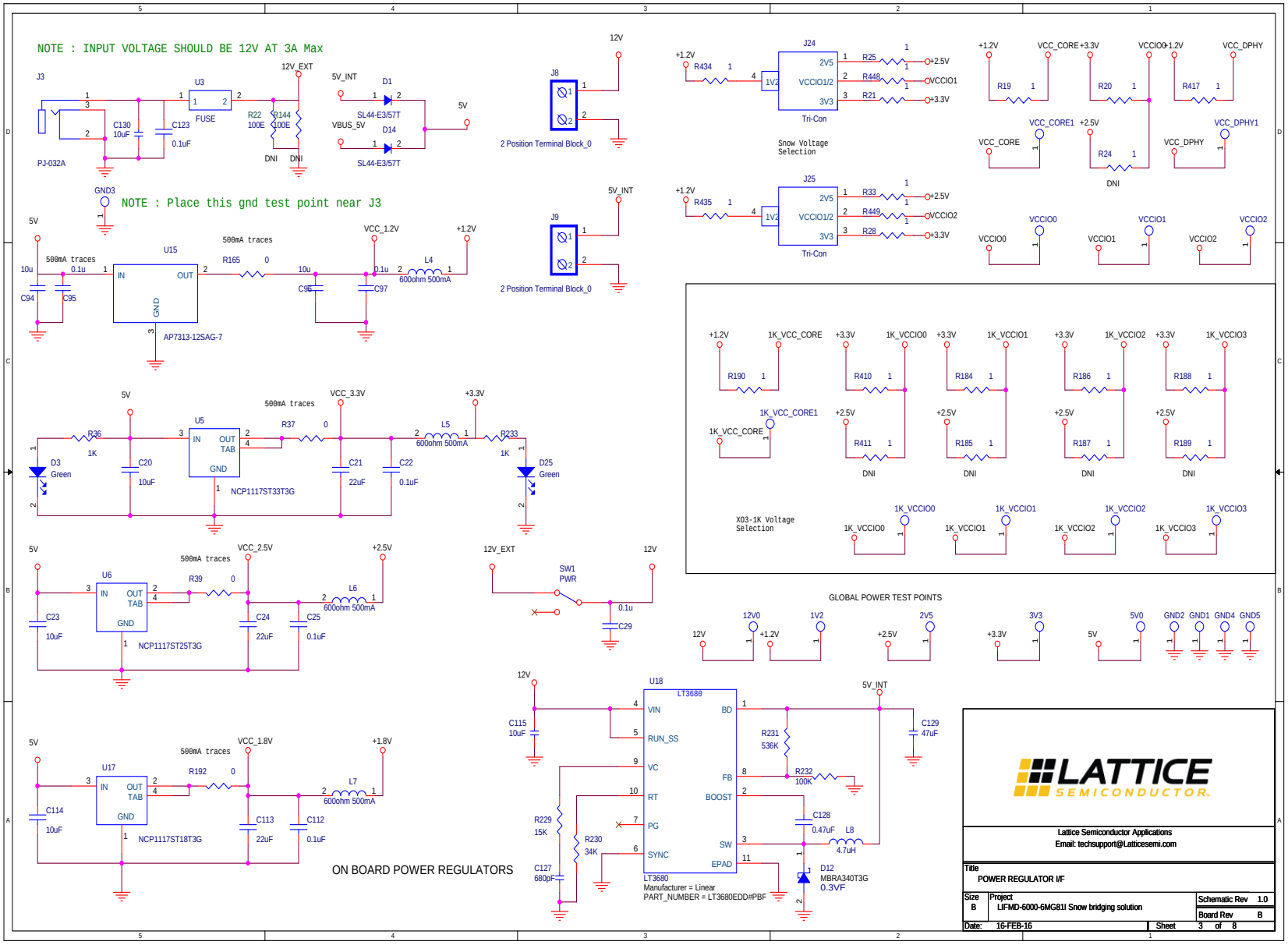
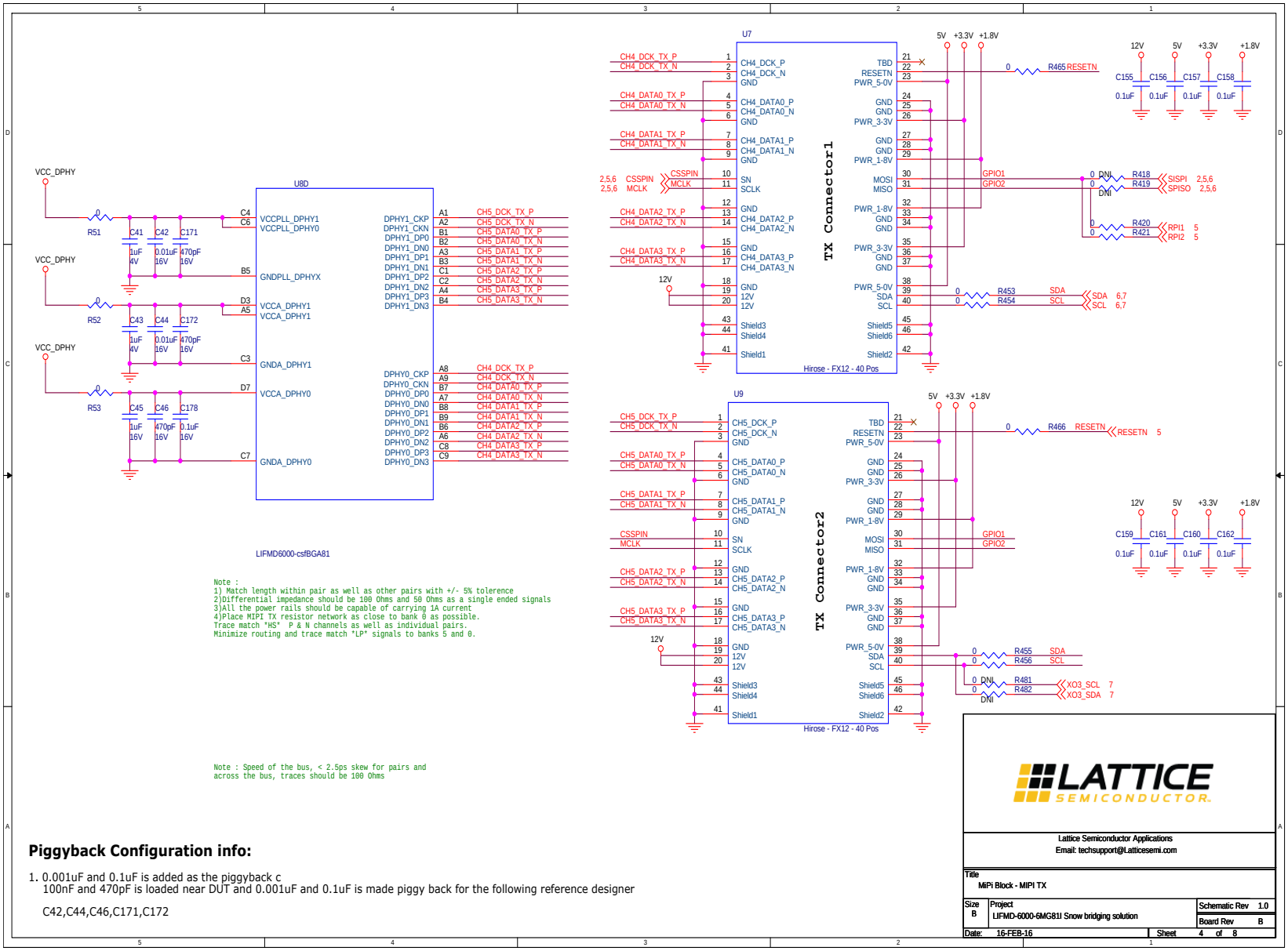


Figure B.3. Power Regulator IF



Piggyback Configuration info:

1. 0.001uF and 0.1uF is added as the piggyback c
   100nF and 470pF is loaded near DUT and 0.001uF and 0.1uF is made piggy back for the following reference designer

   C42,C44,C46,C171,C172

Figure B.4. MIPI Block – MIPI TX

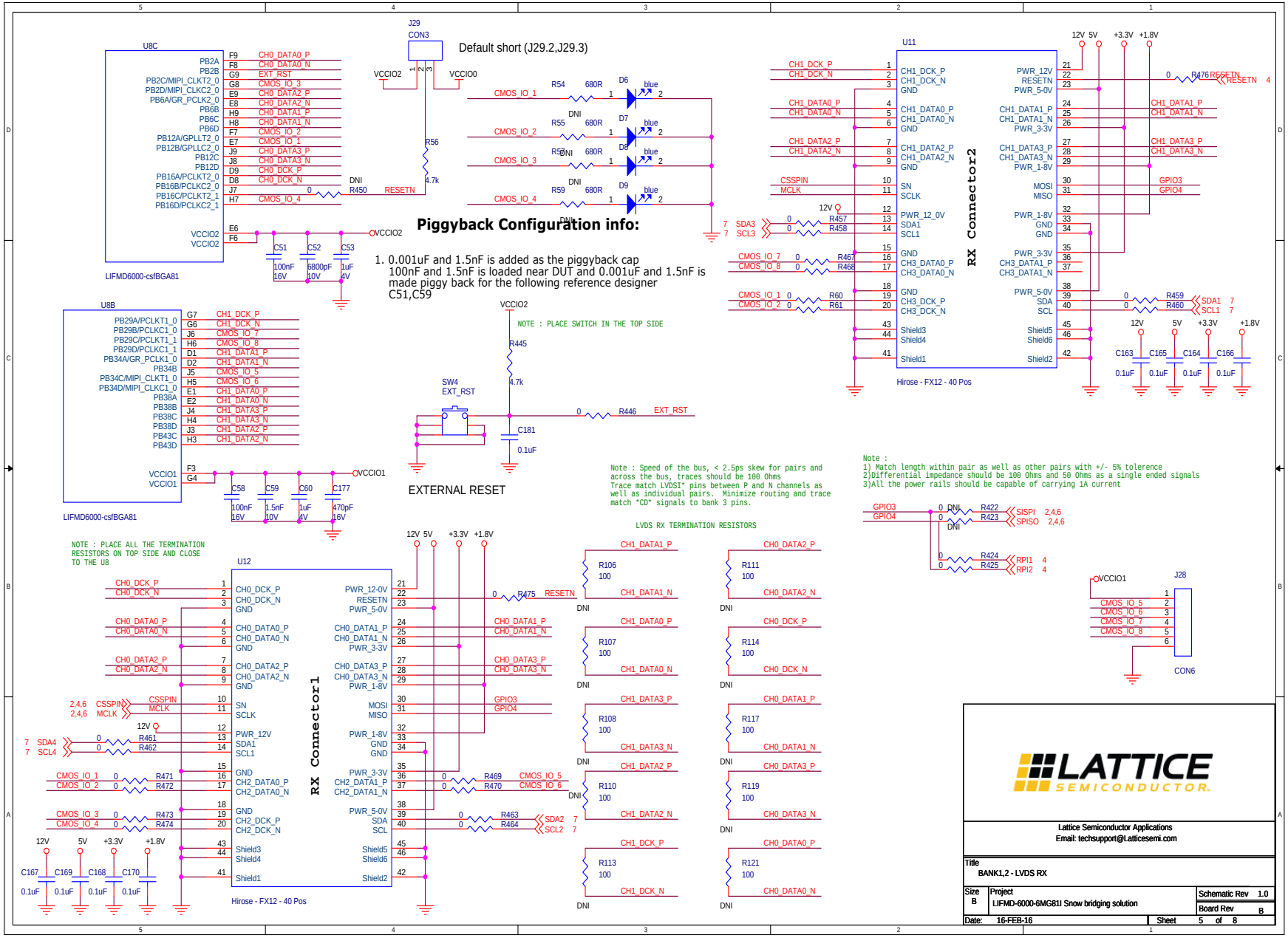


Figure B.5.Bank 1, 2 – LVDS RX

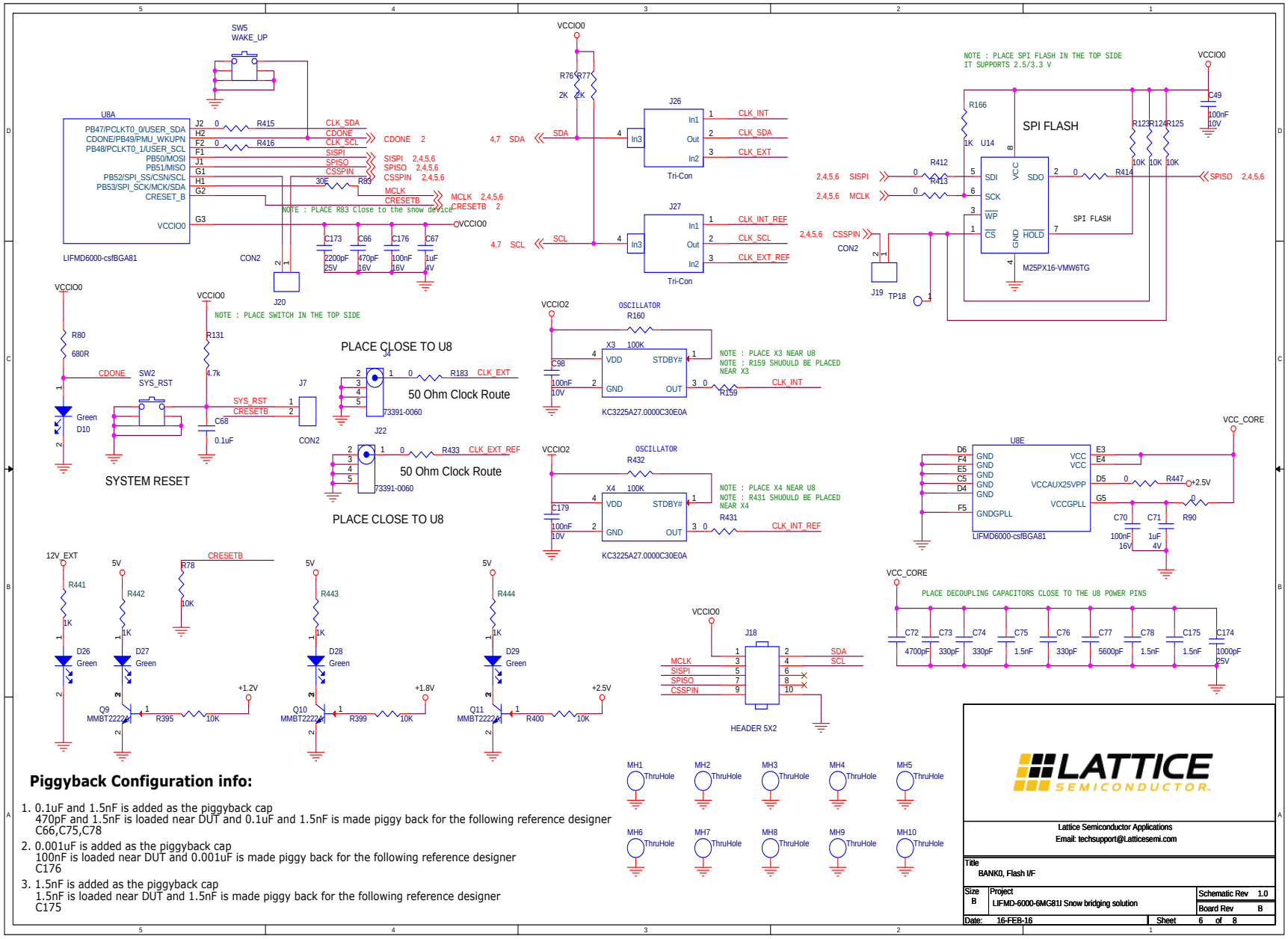


Figure B.6. Bank0 – Flash IF

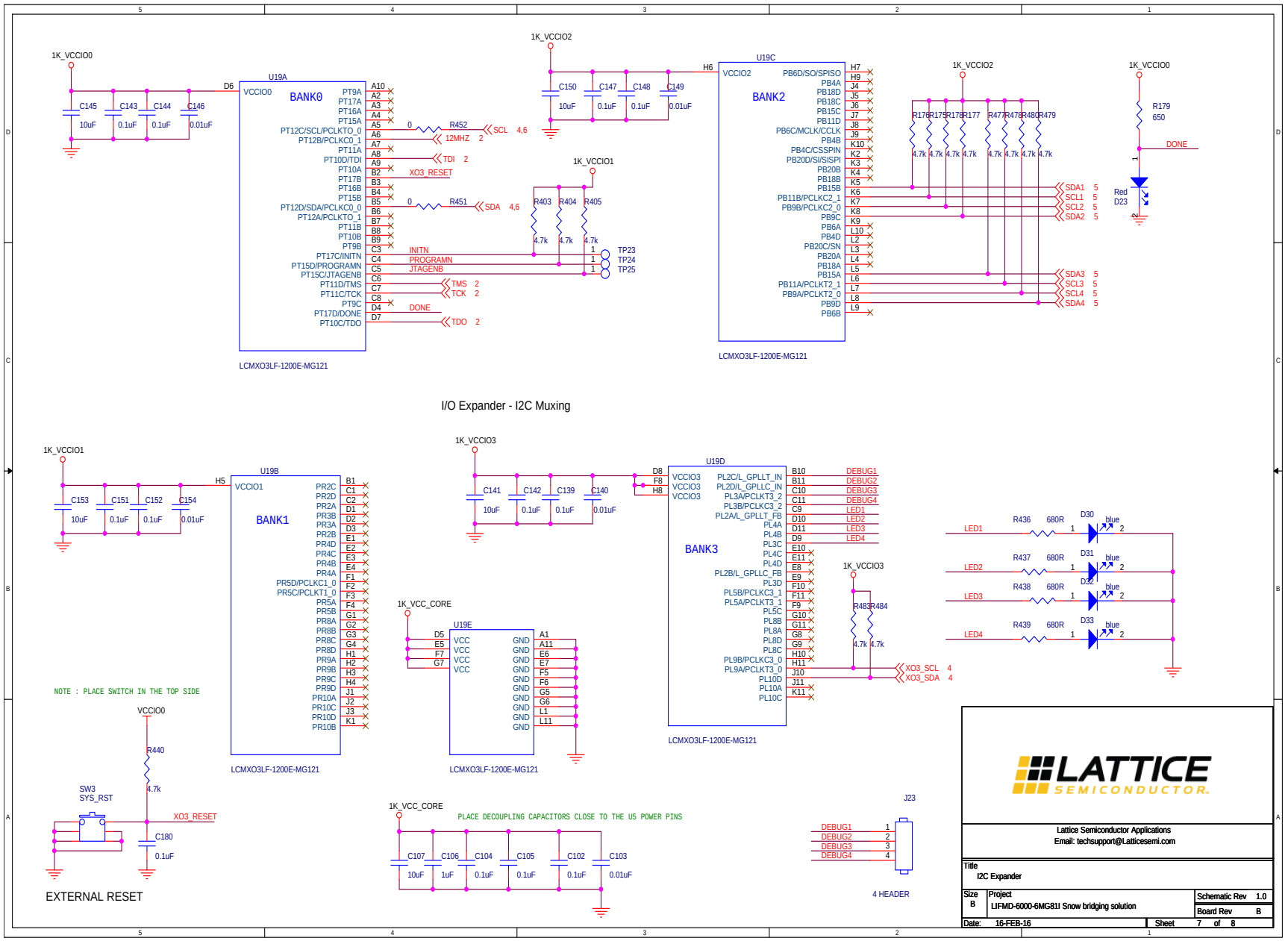


Figure B.7. I²C Expander

Routing guidlines for MIPI & LVDS
---

1)All differential routes are required to have the same length between the positive (true) and the negative (complimentary) routes.
Spacing between the positive (true) and the negative (complimentary) shall be 2 times trace width.

2)Target differential impedance shall be 100 Ohms

3)Trace length matching to be within 1.0 mm (40 mil) across the entire bus.

4)Use small humps for skew corrections

5)Place signal vias close together and remove copper in between vias.
Traces to be fully shielded with GND stitching terminating at both trace end points

6)Board trace impedance results must be within ±10 percent of target and
Power plane impedance to be within +/- 10 percent of target at operating frequency

MIPI &LVDS Simulation Requirement
---

1)MIPI Differential Mode insertion Loss shall be > -1.6dB at 750 MHz

2)MIPI Differential Mode Return Loss shall be < -15dB at 750 MHz

3)MIPI Common Mode Return Loss shall be < -15dB at 750 MHz

4)LVDS differential mode return loss shall be < -16.5db at 600 MHz

5)LVDS common mode return loss shall be < -16.5db at 600 MHz

6)LVDS insertion loss shall be > -1.7db at 600 MHz

7)LVDS Cross coupling shall be < -22 dB for victim IO at 600MHz

8)Power plane impedance to be within +/- 10 percent of target at operating frequency

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Title: Layout Guidelines		
Size: B	Project: LIFMD-6000-6MG81I Snow bridging solution	Schematic Rev 1.0
		Board Rev B
Date: 16-FEB-16	Sheet 8 of 8	

Figure B.8. Layout Guidelines

Appendix C. Raspberry Pi Camera Link Board

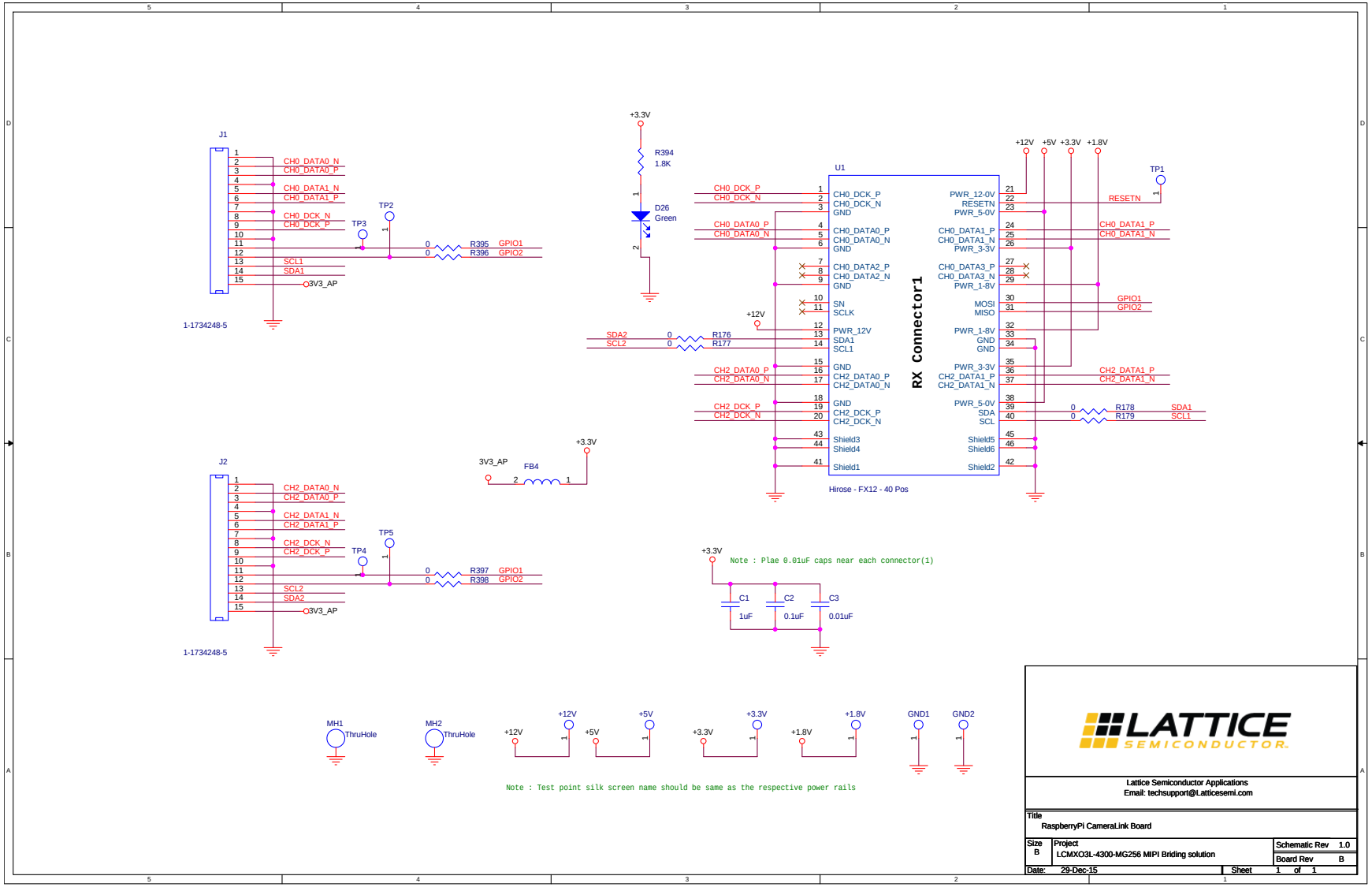

Figure C.9. Raspberry Pi Camera Link Board

Appendix D. Raspberry Pi AP Link Board

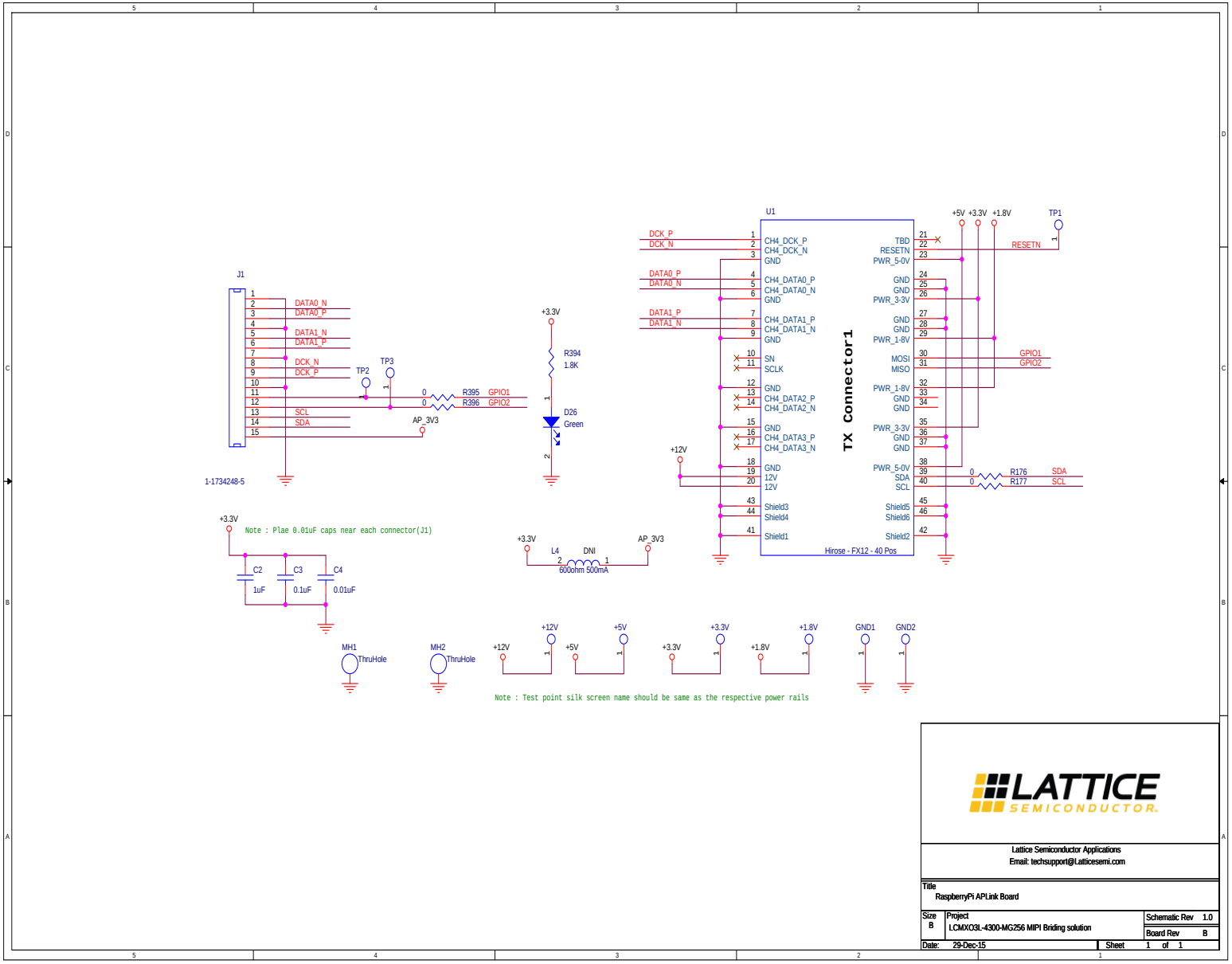

Figure D.10. Raspberry Pi AP Link Board

Revision History

Revision 1.2, August 2018

Section	Change Summary
All	• Changed document number from UG117 to FPGA-UG-02062. • Changed structure of some sections. • Applied minor editorial and formatting changes.
Introduction	Indicated boards as types.
Functional Description	General update
Hardware Setup	Update steps 1, 2, and 6.
Clarity Designer Settings	• Updated Diamond version. • Added steps 5 and 6.
Pinout	General update
I^2C Design	Update introductory paragraph.
Programming Steps	Updated steps 9 and 12.
Appendix A	General update

Revision 1.1, June 2016

Section	Change Summary

All	• Updated Hardware Setup procedure.
	• Added the following sections:
	  • Clarity Designer Settings
	  • Pinout
	  • I2C Design
	• Updated Software Setup procedure.

Revision 1.0, May 2016

Section	Change Summary
All	Initial release.

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