TransFR Usage Guide for Nexus Platform

Technical Note

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Glossary

A glossary of terms used in this document.

Term	Definition
Configuration	The act of writing to volatile configuration memory, such as SRAM, to set the device behavior. Configuration can occur from external sources or via internal transfer from non-volatile memory.
JTAG	Joint Test Action Group. IEEE 1149.1 boundary scan access port for board-level continuity and testing. Also used as an access method to program programmable logic.
FD-SOI (Fully Depleted Silicon On Insulator)	A process that uses an ultra-thin buried oxide layer.
FPGA	Field Programmable Gate Array. A high-density programmable logic device containing small logic cells interconnected through a distributed array of programmable switches.
GOE	Global Output Enable.
GPIO	General Purpose Input/Output pin.
PLL	Phase-Locked Loop. Used in programmable logic for clock management. Common uses include clock multiplication/division and time/phase adjustment.
Programming	The act of writing to non-volatile memory, such as Flash. Configuration can occur directly after programming, or at a later time.
SRAM	Static Random Access Memory. A volatile storage array, generally used in FPGAs for configuration memory.
TransFR	Transparent Field Reconfiguration. A configuration method to allow minimization of system downtime.

1. Introduction

CrossLink™-NX and Certus™-NX family of low-power FPGAs can be used in a wide range of applications, and are optimized for bridging and processing needs in the Embedded Vision space. It is built on Lattice Nexus FPGA platform, using low-power 28-nm FD-SOI technology.

One of the fundamental benefits of using an FPGA is the ability to reconfigure its functionality without removing the device from the system. Numerous mechanisms of providing field updates have been implemented. Access to the system FPGA can be as simple as a direct cable connection or something as complex as remote access using wireless links. Current update methods generally require a significant disruption to the system during the configuration update. It is desirable to reduce or eliminate the downtime resulting from reconfiguration due to an update, especially for non-redundant and mission-critical equipment.

Lattice provides TransFR™ (Transparent Field Reconfiguration) Technology to support reconfiguration with minimal system interruptions. TransFR support is enabled through Lattice Radiant® Software in the reconfiguration bitstream.

2. TransFR Technology

TransFR is a Lattice unique technology that allows the FPGA to be updated in the field with minimum interruption to the system operation by freezing the I/O states during device re-configuration with the new bitstream. TransFR is supported for both JTAG and non-JTAG port configurations. JTAG port configuration controls the I/O through BSCAN (Boundary Scan) register. Non-JTAG port configuration controls the I/O through bit 28 of Control Register 0.

3. Boundary Scan Control

CrossLink-NX and Certus-NX devices provide a four-pin JTAG engine that is fully compliant with IEEE 1149.1 and IEEE 1532 standards. IEEE 1149.1 is the standard for Test Access Port and Boundary-Scan Architecture. IEEE 1532 is the standard for In-System Configuration of Programmable Devices. The boundary-scan (BSCAN) cells have the ability to be sampled and preloaded, allowing controllable I/O behavior during configuration. The JTAG Test Access Port is enabled when JTAG_EN pin equals to *1*. The four shared pins become TDI, TDO, TCK, and TMS. The Test Access Port power is supplied through VCCIO1.

4. JTAG Mode TransFR

Following is a detailed description of JTAG mode TransFR.

Phase 1: The external Flash memory is reprogrammed through the JTAG port while the SRAM is running undisturbed, allowing the system to continue operating without any disruptions.

Phase 2: I/O states are frozen and the outputs retain these levels throughout the reconfiguration process. This effectively pauses the FPGA, keeping any critical control and status outputs in their desired states during the system update.

Phase 3: While the I/O states are frozen, JTAG commands are used to initiate the transfer of the new bitstream from external Flash to the SRAM configuration space. After the SRAM is configured, I/O is released. The GSR signal is asserted internally to place the CrossLink-NX/Certus-NX device into a predictable state. After reconfiguration has completed and prior to the exit of boundary-scan mode in Phase 4, the internal device logic is actively interpreting the input signals. This time period can be used for a number of purposes to allow for a custom reactivation. Common uses include:

- Synchronization of PLLs to incoming clock sources
- Manipulation of event counters and state machines into desired operational states
- Ensuring status and error indicators are properly initialized

Phase 4: I/O settings are released after completion of configuration. The internal logic seamlessly assumes control of the I/O.

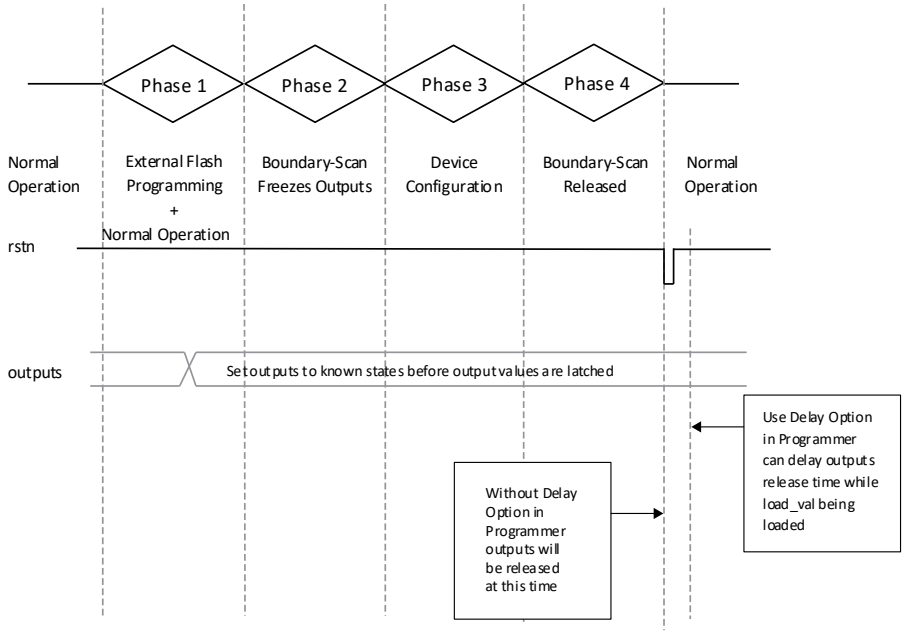

Figure 4.1. Example JTAG Mode TransFR Sequence

5. Non-JTAG Mode TransFR

Following is a detailed description of non-JTAG mode TransFR.

Phase 1: The external Flash memory is reprogrammed through the sysCONFIG SPI port while the SRAM is running undisturbed, allowing the system to continue operating without any disruption.

Phase 2: CrossLink-NX/Certus-NX device starts to refresh. I/O states are captured and held into the I/O latches. Outputs retain these levels throughout the reconfiguration process. This effectively pauses the FPGA, keeping any critical control and status outputs in their desired states during the system update.

Phase 3: I/O remains under the control of I/O latches while the new bitstream transfers from external Flash memory to SRAM configuration space.

Phase 4: I/O is released from I/O latch to user function only when Global Output Enable (GOE) is released during wakeup stage. To maintain all output states after device wake up, resetting on the output registers needs to be done prior to wake up. For example, if the design involves GSR, then asserting GSR could reset all the output registers.

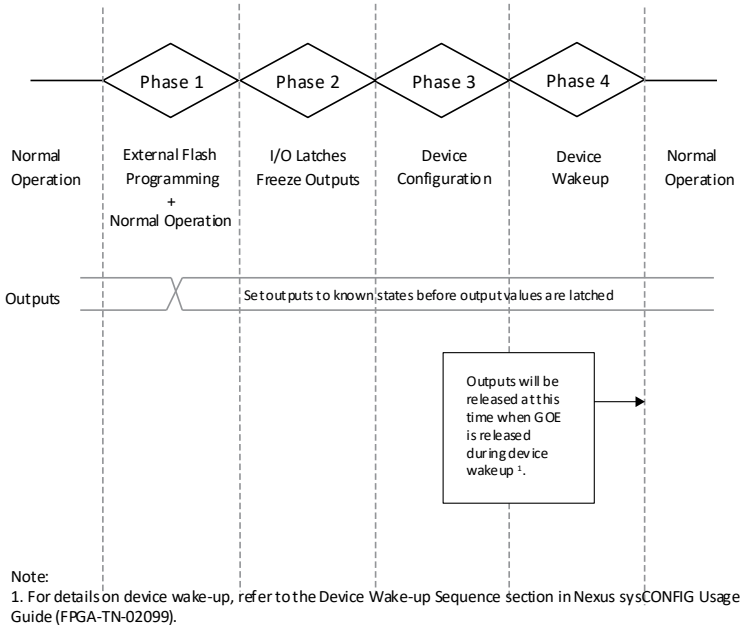

Figure 5.1. Example Non-JTAG Mode TransFR Sequence

6. TransFR Flow with Lattice Radiant Software

TransFR preference for CrossLink-NX and Certus-NX devices can be enabled/disabled through the Lattice Radiant Software. The TRANSFR preference is listed in the Device Constraint Editor (Figure 6.1) under the Global tab. This needs to be enabled in the new bitstream pattern that is going to be programmed into the external Flash.

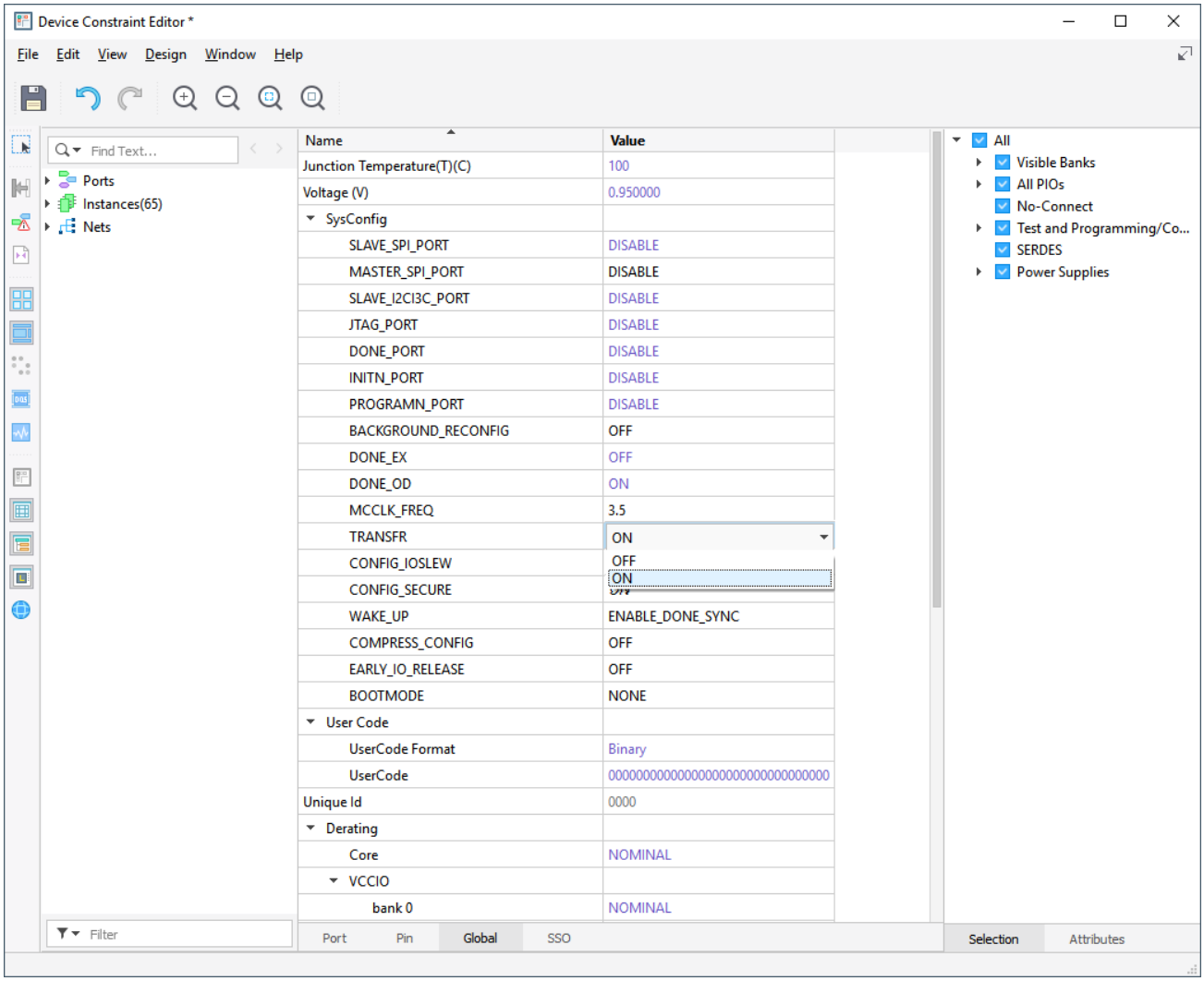

Figure 6.1. Lattice Radiant Software: Device Constraint Editor – TRANSFR

Once the TransFR bitstream is generated, it needs to be programmed into the external Flash. This is done through the Radiant Programmer. Figure 6.2 shows the configuration of an external Macronix SPI Flash using the JTAG port. Figure 6.3 shows the configuration of an external Macronix SPI Flash using the SPI port. The reconfiguration process for TransFR is initiated via refresh command or by toggling PROGRAMN pin.

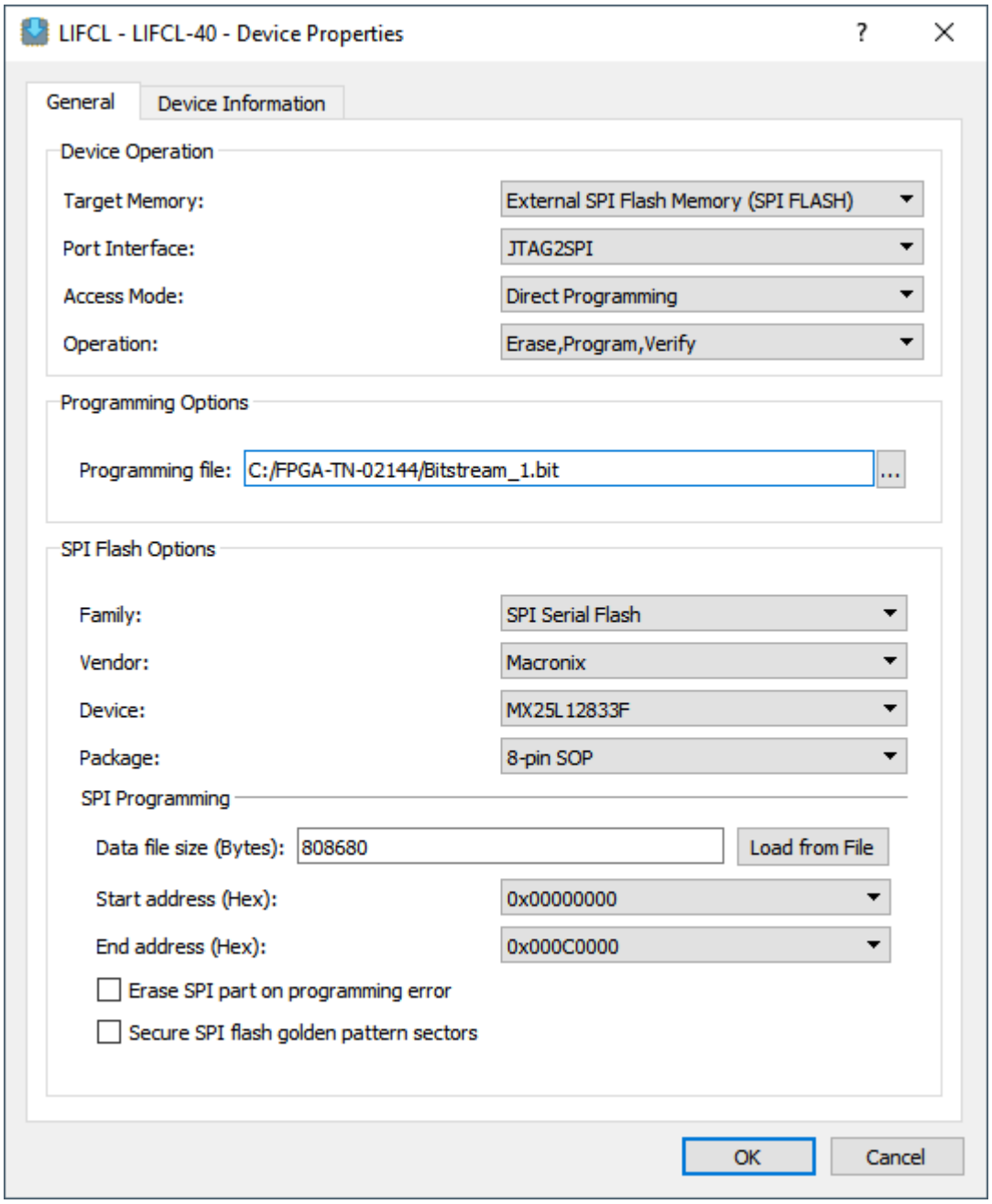

Figure 6.2. Radiant Programmer – External SPI Flash Programming through JTAG

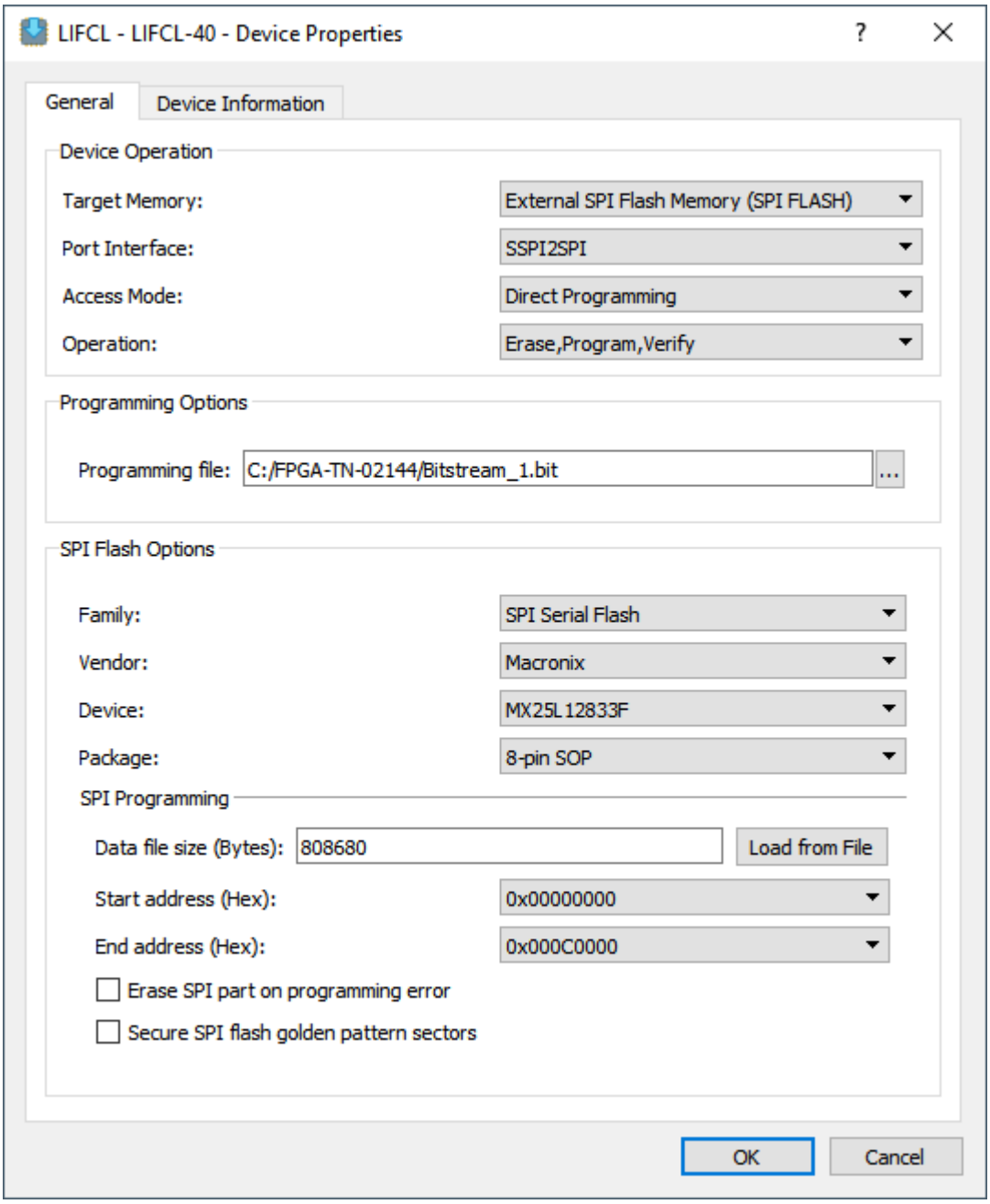

Figure 6.3. Radiant Programmer – External SPI Flash Programming through SPI

References

For more information, refer to the following documents:

- CrossLink-NX Family Data Sheet (FPGA-DS-02049)
- Nexus sysCONFIG Usage Guide (FPGA-TN-02099)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.1, June 2020

Section	Change Summary
All	Changed the document title to TransFR Usage Guide for Nexus Platform.
Introduction	Added support for the Nexus platform including Certus-NX and CrossLink-NX device families.
Boundary Scan Control	
JTAG Mode TransFR	
Non-JTAG Mode TransFR	
TransFR Flow with Lattice Radiant Software	

Revision 1.0, December 2019

Section	Change Summary
All	Production release.

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