I3C Configuration Cable Bridge Prototype User Guide

Usage Guide

FPGA-AN-02055-1.1

July 2022

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults and associated risk the responsibility entirely of the Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Contents

Acronyms in This Document 5
1. Introduction 6
1.1. Quick Facts 6
1.2. Features 7
1.3. Conventions 7
1.3.1. Definition of Terms 7
1.3.2. Hardware Requirement 7
2. Functional Description 8
2.1. Overview 8
2.2. Cable Connection 8
3. I3C Configuration Cable Bridge Setup 9
3.1. Programming Cable 9
3.2. I3C Configuration Cable Bridge IP Board 9
3.3. Bridge Board Connection 11
4. Target Device Programming 12
4.1. Radiant Programmer GUI Setup 12
4.2. Radiant Programmer Operation Options 13
5. Timing Diagram 14
6. Limitation 15
Appendix A. Bridge Board Setup 16
A.1. Connector Installation 16
A.2. Board Programming 16
References 17
Technical Support Assistance 18
Revision History 19

Figures

Figure 2.1. I3C Configuration Cable Bridge Functional Diagram 8
Figure 2.2. I3C Configuration Cable Bridge Connection 8
Figure 3.1. USB Cable – HW-USBN-2B 9
Figure 3.2. iCE40UP Breakout Board (Top View) 10
Figure 3.3. Programming Cable and Programming Device Connection 11
Figure 4.1. Radiant Programmer Setup for Programming 12

Figure A. 1. Header Installation 16

Tables

Table 1.1. Quick Facts 6
Table 3.1. Board Connection – Functionality Assignment 10
Table 3.2. Board Connection – Specific Pin Assignment 11
Table 4.1. Radiant Programmer Operation Options 13

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
GND	Ground
IP	Intellectual Property
LUT	Lookup-Table
SPI	Serial Peripheral Interface
I3C	Improved Inter-Integrated Circuit
SDA	Serial Data
SCL	Serial Clock
GPIO	General Purpose Input/Output

1. Introduction

For Lattice Nexus Platform devices, the I3C Configuration Cable Bridge provides an interface with bridging logic to covert HW-USBN-2B data traffic into I3C bus format, hence allows Lattice Radiant Programmer 3.2 (and later) to access Lattice FPGA configuration logic via the I3C configuration interface. This bridge is built on Lattice iCE40 UltraPlus Breakout Board (iCE40UP5K-B-EVN) which serves as the bridging element between Lattice USB Download Cable HW-USBN-2B and Lattice Nexus Platform devices.

1.1. Quick Facts

Table 1.1 presents a summary of SPI to the I3C Configuration Interface Bridge Soft IP Core.

Table 1.1. Quick Facts

Hardware Requirements	I3C Configuration Bridge Platform	iCE40 UltraPlus Breakout Board (iCE40UP5K-B-EVN)
	Lattice USB Download Cable	HW-USBN-2B
	I3C Cable	Contains three wires, for SCL, SDA and GND connection
Software Requirements	Supported User Interfaces	Lattice Radiant Programmer 3.2 (and later)
Device Requirements	Targeted Device	Nexus Platform Device families

The I3C Configuration Cable Bridge IP utilizes the I3C ENTDAA CCC command to achieve the dynamic address assignment. By default, the slave address 7'h70 is assigned to the targeted Nexus slave I3C configuration port, which is used by Lattice Radiant Programmer to communicate with the targeted Nexus device. This SPI-I3C Configuration Cable Bridge solution supports an I3C bus containing a single Nexus device. Multiple Nexus devices are not supported.

1.2. Features

I3C bus speed is at 12 MHz.

1.3. Conventions

1.3.1. Definition of Terms

This document uses the following terms to describe common functions:

Configuration – Configuration refers to a change in the state of the Nexus Platform Device memory cells.

1.3.2. Hardware Requirement

To achieve Nexus Platform Device programming through I3C Configuration Interface, following hardware are required:

- iCE40 UltraPlus Breakout Board iCE40UP5K-B-EVN programmed with I3C Configuration Cable Bridge IP;
- Lattice USB Download Cable HW-USBN-2B;
- I3C Cable which contains three wires for SCL, SDA and GND connections.

2. Functional Description

2.1. Overview

I3C Configuration Cable Bridge connects the Lattice HW-USBN-2B Cable to the Slave I3C configuration interface of the targeted Nexus devices.

I3C Configuration Interface Bridge functional diagram is shown in Figure 2.1.

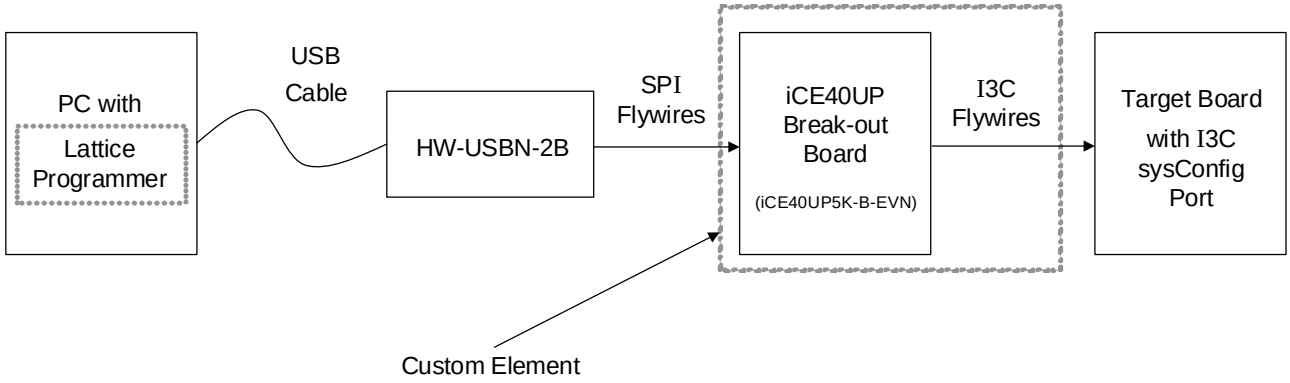

Figure 2.1. I3C Configuration Cable Bridge Functional Diagram

2.2. Cable Connection

The cable connections are demonstrated in Figure 2.2.

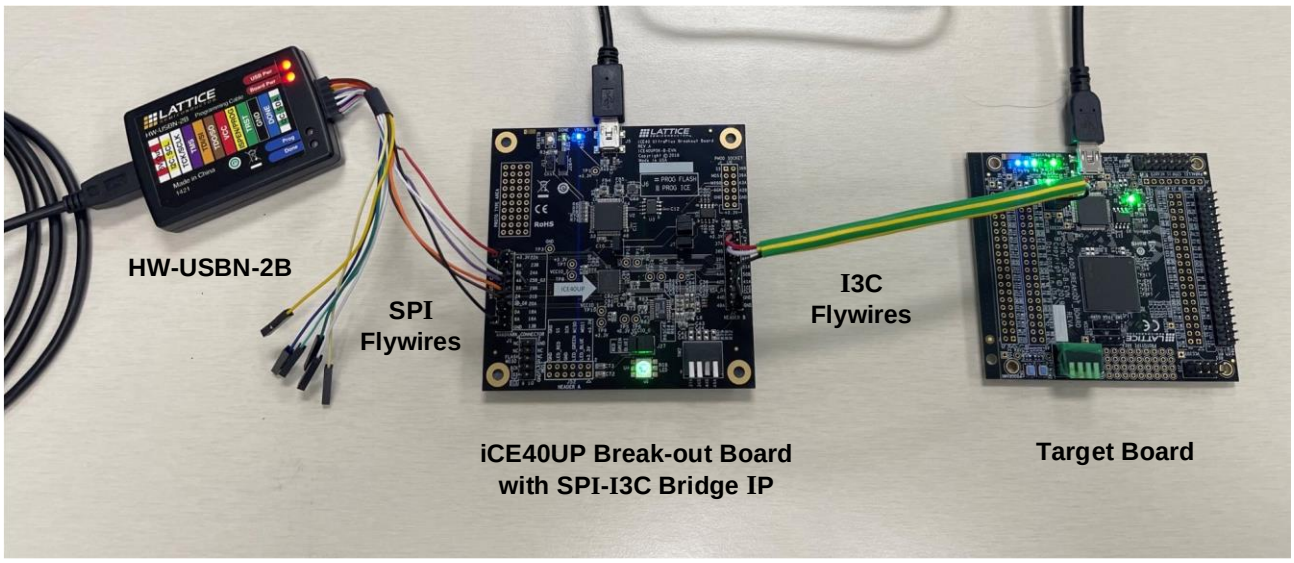

Figure 2.2. I3C Configuration Cable Bridge Connection

3. I3C Configuration Cable Bridge Setup

This section provides information on how to setup the I3C Configuration Cable Bridge, including using Lattice Radiant Programmer to achieve the Nexus devices programming. For more details on Radiant Programmer, refer to the Lattice Radiant Software 3.2 User Guide.

3.1. Programming Cable

I3C Configuration Cable Bridge utilizes the Lattice HW-USBN-2B to achieve the Nexus device programming, as shown in Figure 3.1 below.

Figure 3.1. USB Cable – HW-USBN-2B

For detailed information regarding the HW-USBN-2B, refer to Programming Cable User Guide (FPGA-UG-02042).

3.2. I3C Configuration Cable Bridge IP Board

The I3C Configuration Cable Bridge IP is targeted and programmed into the iCE40UP Breakout Board. The top view of the iCE40UP Breakout Board is shown in Figure 3.2 below. For more details about the iCE40UP Breakout Board, refer to iCE40 UltraPlus Breakout Board User Guide (FPGA-UG-02001).

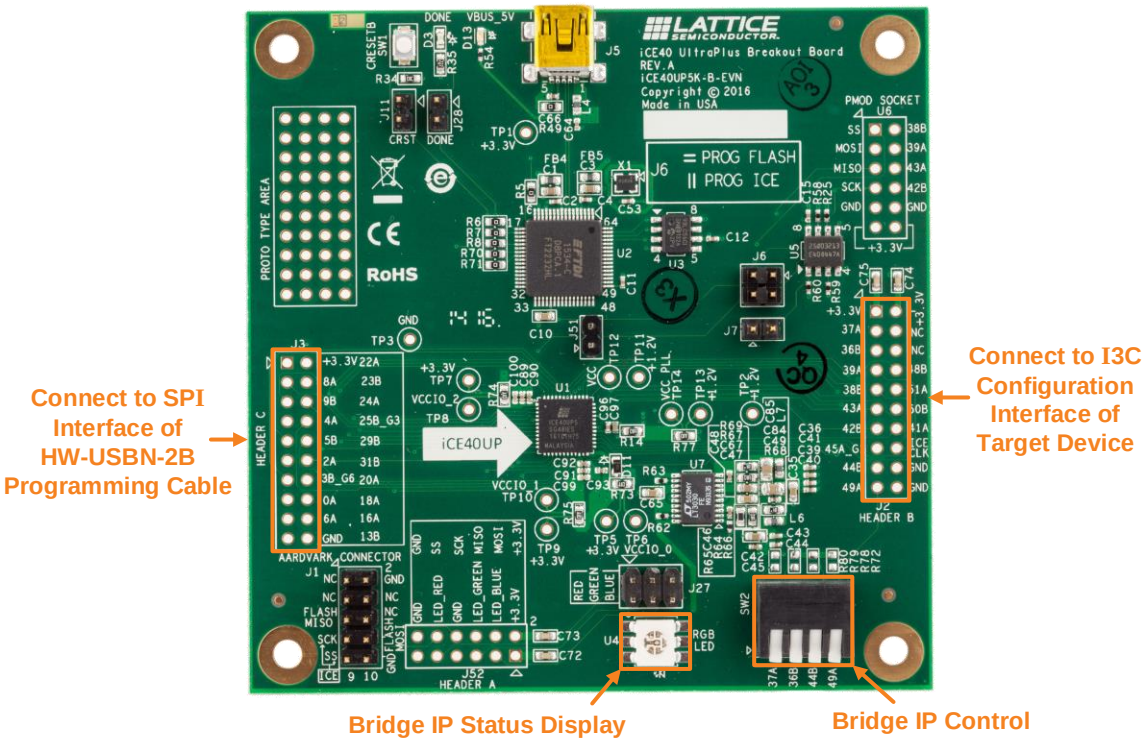

Figure 3.2. iCE40UP Breakout Board (Top View)

Header C is used to connect to the HW-USBN-2B Programming Cable. Header B is used to connect to the I3C Configuration Interface of the target Nexus device. Refer to Table 3.2 for specific pin assignments.

The DIP Switches SW2 is used for Bridge control. Refer to Table 3.1 for the functionality assignments.

Table 3.1. Board Connection – Functionality Assignment

DIP Switches	Board Marking	Function
SW2-1	37A	Unused. Must in OFF position due to the pin sharing scheme on the board.
SW2-2	26B	Unused. Must in OFF position due to the pin sharing scheme on the board.
SW2-3	44B	Serves as RGB LED Brightness control, OFF = Full Brightness, ON = Half Brightness.
SW2-4	49A	Serves as IP Reset, which is edge sensitive with ~250ns debounce.

Note: "OFF" refers to the 'UP' position. "ON refers to the "DOWN" position.

The RGB LED is used for IP status display:

- RED LED: Blinking = IP is busy initialization; Breathing = IP is busy setting up I3C Transaction.
- GREED LED: Breathing = IP is idle.
- BLUE LED: Breathing = SPI port is busy receiving/transmitting data.

The RGB LED blinking or breathing for busy status is triggered by the rising edge of the corresponding internal busy flag. The durations are only for visual observability, not reflect the real busy time.

3.3. Bridge Board Connection

The iCE40UP Breakout Board with SPI to I3C Configuration Interface Bridge IP should be connected to the Lattice Programming cable (HW-USBN-2b) as shown in Figure 3.3 below.

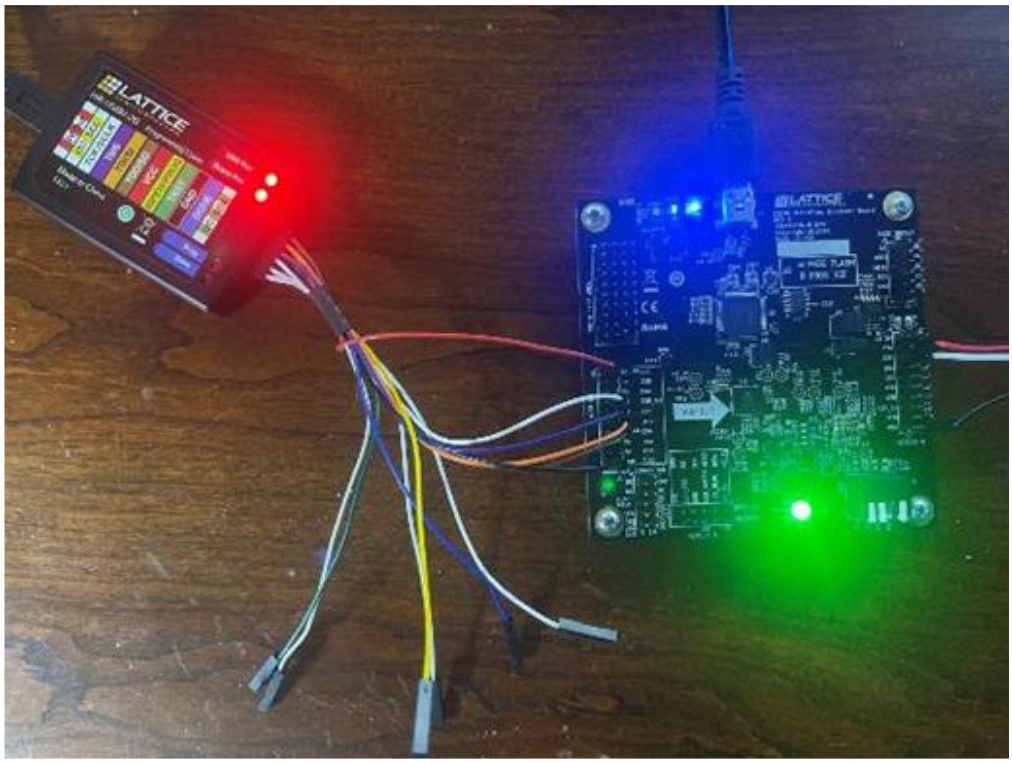

Figure 3.3. Programming Cable and Programming Device Connection

Detailed connection information is listed in Table 3.2 below.

Table 3.2. Board Connection – Specific Pin Assignment

HW-USBN-2B		iCE40UP Breakout Board				Target Nexus Board
Signal Name	**Wire Color**	**Header**	**Pin**	**Board Marking**	**IP Signal Name**	**Signal Name**
VCC	RED	Header C (J3)	1	+3.3V	—	—
GND	BLACK	Header C (J3)	19	GND	—	—
TCK/SCLK	WRITE	Header C (J3)	8	25B_G3	SCLK	—
TMS/SCSN	PURPLE	Header C (J3)	10	29B	SSn	—
TDI/SI	ORANGE	Header C (J3)	12	31B	SI	—
TDO/SO	BROWN	Header C (J3)	14	20A	SO	—
—	—	Header B (J2)	20	GND	—	GND
—	—	Header B (J2)	3	37A	scl	SCL
—	—	Header B (J2)	5	36B	sda	SDA

Note: The JTAG_ENABLE pin for the targeted Nexus device must be driven low when performing SSPI-I3C programming.

4. Target Device Programming

To program the targeted Nexus device, you need to use Lattice Radiant Programmer Rev 3.2 (or later).

4.1. Radiant Programmer GUI Setup

Launch Radiant Programmer. As shown in Figure 4.1 below, choose the **Edit > Device Properties**… menu item, or click the Operation area. From the prompted Device Properties dialog, choose *I3C Bridge* from the drop-down menu of the Port Interface.

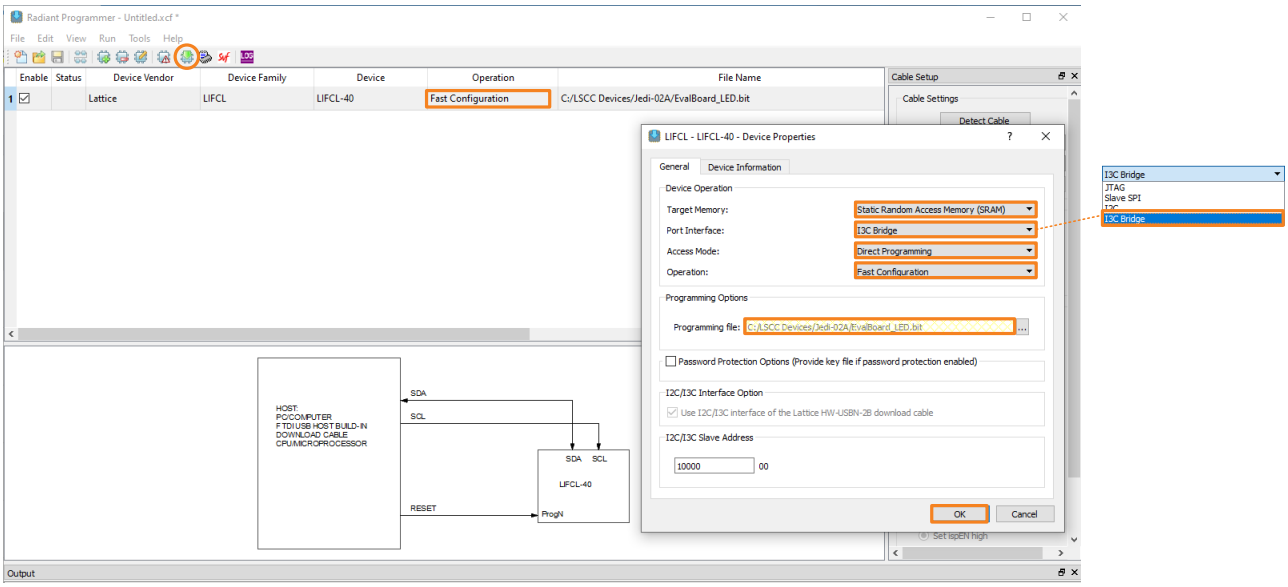

Figure 4.1. Radiant Programmer Setup for Programming

Finish the settings with desired **Target Memory**, **Access Mode** and **Operation**. Click **OK**. Click the **Program Device** icon from the toolbar to perform the device programming.

4.2. Radiant Programmer Operation Options

The Radiant Programmer operation options are summarized in Table 4.1 below.

Table 4.1. Radiant Programmer Operation Options

Target Memory	Static Random Access Memory (SRAM)		Non-Volatile Configuration Memory	
Port Interface	**I3C Bridge**		**I3C Bridge**	
Access Mode	**Direct Programming**	**Background Programming**	**Feature Row Programming**	**Advanced Security Keys Programming**
Operation	Fast Configuration	SEI Fast Program	Program Feature Row	Program Password Key
	Erase, Program, Verify	Verify Only	Update Feature Row	Read Password Key
	Verify Only	Verify ID	Read Feature Row	Program Encryption Key
	Erase Only	Display ID	Program Control NV Register 1	Read Encryption Key
	Verify ID	Display USERCODE	Display Control NV Register 1	Program Public Key
	Display ID	Display Control Register0	—	Read Public Key
	Display USERCODE	Display Control Register1	—	Program TraceID
	Display Control Register0	Read Status Register	—	Display TraceID
	Program Control Register0	Refresh	—	Program Lock Policies
	Display Control Register1	External Primary Dry Run	—	Read Lock Policies
	Program Control Register1	External Golden Dry Run	—	—
	Program DONE bit	Bypass	—	—
	Read Status Register	—	—	—
	Refresh	—	—	—
	External Primary Dry Run	—	—	—
	External Golden Dry Run	—	—	—
	Bypass	—	—	—

5. Timing Diagram

I3C bus timing and timing diagrams are described in Specification for I3C from MIPI Alliance.

6. Limitation

There are some limitations for current I3C Configuration Cable Bridge support:

- The *Read and Save* operation is not supported in I3C Configuration Cable Bridge. *Verify* operation is supported with Software workaround.
- Limited validation testing for I3C Configuration Cable Bridge has been performed for Radiant Programmer Rev 3.2. Full validation is to be performed for official Radiant Programmer Rev 3.2 release.
- Lattice Nexus devices do not support bridging from the Slave I3C port to the Master SPI port. Supported operations are limited to SRAM and Non-volitile configuration bits, per Table 4.1. External SPI Flash operations are supported via JTAG and SSPI sysConfig ports, if desired.

Appendix A. Bridge Board Setup

If additional I3C Cable Bridge prototype hardware is needed, follow the instructions below to set up a standard iCE40 UltraPlus Breakout Board (ICE40UP5K-B-EVN) for I3C Configuration Cable Bridge application. The steps involve soldering connectors on the board and programming the SPI Flash (Micron, N25Q032A13ESC40F) on the board.

A.1. Connector Installation

Install the 2×10 headers (Samtec MTSW-110-08-T-D-300) for J2 (Header B) and J3 (Header C) as shown in Figure A. 1 below.

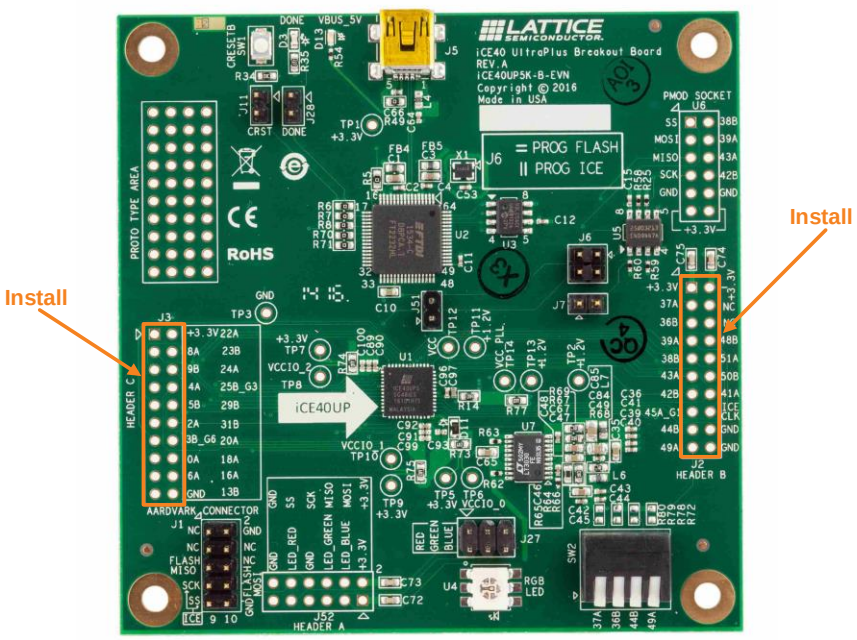

Figure A. 1. Header Installation

A.2. Board Programming

Program the iCE40UP Breakout Board with bitstream file (SPI_I3C_Bridge_impl_1.bin) provided by following the instructions in the Board Configuration and Programming section of the iCE40 UltraPlus Breakout Board User Guide (FPGA-UG-02001).

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see Lattice Radiant Software 3.2 User Guide.

- iCE40 Programming and Configuration (FPGA-TN-02001)
- iCE40 UltraPlus Breakout Board User Guide (FPGA-UG-02001)
- Programming Cable User Guide (FPGA-UG-02042)
- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- Specification for I3C from MIPI Alliance

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.1, July 2022

Section	Change Summary
All	Newly added the Bridge Board Setup section.
Introduction	Added description regarding dynamic address assignment to the Quick Facts section.

Revision 1.0, July 2022

Section	Change Summary
All	Production release.

www.latticesemi.com