AXI Registers for Custom IP Framework — Lattice Propel Builder

User Guide

FPGA-IPUG-02221-1.0

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AMBA	Advanced Micro-controller Bus Architecture
AXI	Advanced Extensible Interface Bus
FPGA	Field Programmable Gate Array
IP	Intellectual Property
RTL	Register Transfer Level

1. Introduction

The Lattice Semiconductor AXI Registers for Custom IP Framework is used as a skeletal framework for creation of a custom IP that uses register resources and AXI4 as the bus interface. It simply generates the configured number of registers, and all addressable registers are connected to an AXI4 (or AXI4-Lite) Subordinate Interface where it can perform Write and Read transactions.

1.1. Quick Facts

Table 1.1 presents a summary of the AXI Registers for Custom IP Framework.

Table 1.1 AXI Registers for Custom IP Framework Quick Facts

IP Requirements	Supported FPGA Families	Lattice Avant™, CertusPro™-NX
Resource Utilization	Targeted Devices	LAV-AT-500E, LFCPNX-100
	Supported User Interface	AXI4, AXI4-Lite
	Resources	See Table A.2 and Table A.3.
Design Tool Support	Lattice Implementation	Lattice Propel™ Builder Software – IP Configuration, Generation, and Implementation Lattice Radiant™ Software – Synthesis, Map, Place and Route
	Synthesis	Synopsys® Synplify Pro® for Lattice
	Simulation	For a list of supported simulators, see the Lattice Radiant software user guide.

1.2. Features

The key features of this AXI Registers for Custom IP Framework IP include:

- Compliance with AMBA AXI4/AXI4-Lite protocol
- Supports configurable interface type between AXI4 and AXI4-Lite
- Configurable number of registers: 4 to 1024
- Configurable interface data width: 8, 16, 32, 64, 128, and 256
- Configurable interface address width: 12 to 32 bits
- Supports AXI4 INCR burst type only
- Supports narrow write and read transactions
- Supports unaligned address transactions
- Single AXI4 Subordinate Interface implementation
- Configurable Base Address and Address Space of IP

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals
- *_io* are bidirectional input/output signals

1.3.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Descriptions

2.1. Overview

The Lattice Semiconductor AXI Registers for Custom IP Framework simply generates the configured number of registers. All addressable registers are connected to an AXI4 (or AXI4-Lite) Subordinate Interface where it can perform Write and Read transactions. It is mainly used as a base design for a custom logic that requires register resources and AXI4 as the interface.

The generated IP contains the configured number of registers and the AMBA AXI4 Protocol implementation. Other optional modifications or additions by the user can be done by manually editing or using the generated RTL file.

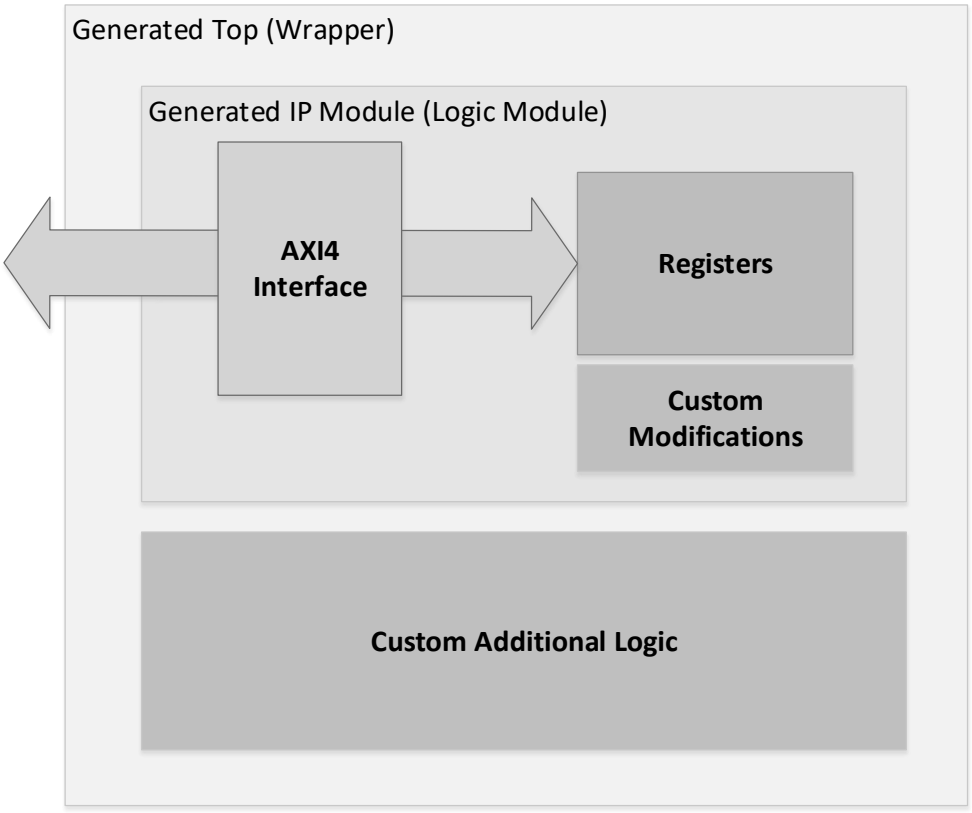

Figure 2.1. Skeletal Framework for IP Creation with AXI Registers Implementation

2.2. Signals Description

Table 2.1 shows all the initial ports for this IP, which are basically the AXI protocol signals.

Table 2.1. Signals Description

Pin Name	Direction	Width (Bits)	Description
Clock and Reset			
aclk_i	In	1	AXI and registers clock.
aresetn_i	In	1	Active low reset.
AXI4			
axi_s0_awvalid_i	In	1	Write address valid. This signal indicates that the channel is signaling valid write address and control information.
axi_s0_awaddr_i	In	AXI_ADDR_WIDTH	Write address. The write address gives the address of the first transfer in a write burst transaction.
axi_s0_awsize_i	In	3	Burst size. This signal indicates the size of each transfer in the burst. AXI4-Lite: N/A
axi_s0_awburst_i	In	2	Burst type. The burst type and the size information, determine how the address for each transfer within the burst is calculated. AXI4-Lite: N/A
axi_s0_awlen_i	In	8	Burst length. This indicates the number of beats per AXI burst. AXI4-Lite: N/A
axi_s0_awid_i	In	AXI_ID_WIDTH	AXI write ID width.
axi_s0_awlock_i	In	1	Lock type. AXI4: Optional AXI4-Lite: N/A
axi_s0_awcache_i	In	4	Memory type. AXI4: Optional AXI4-Lite: N/A
axi_s0_awprot_i	In	3	Protection type. AXI4: Optional AXI4-Lite: Optional
axi_s0_awqos_i	In	4	Quality of Service. AXI4: Optional AXI4-Lite: N/A
axi_s0_awregion_i	In	4	Region. AXI4: Optional AXI4-Lite: N/A
axi_s0_awuser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional AXI4-Lite: N/A
axi_s0_awready_o	Out	1	Write address ready. This signal indicates that the subordinate is ready to accept an address and associated control signals.
axi_s0_wvalid_i	In	1	Write valid. This signal indicates that valid write data and strobes are available.

Pin Name	Direction	Width (Bits)	Description
axi_s0_wdata_i	In	AXI_DATA_WIDTH	Write data.
axi_s0_wlast_i	In	1	Write last. This signal indicates the last transfer in a write burst.
axi_s0_wuser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional. AXI4-Lite: N/A
axi_s0_wstrb_i	In	AXI_DATA_WIDTH/8	Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus.
axi_s0_wready_o	Out	1	Write data ready. This signal indicates that the subordinate is ready to accept write data.
axi_s0_bvalid_o	Out	1	Write response valid. This signal indicates that the channel is signaling a valid write response.
axi_s0_bid_o	Out	AXI_ID_WIDTH	Write response ID.
axi_s0_bresp_o	Out	2	Write response. This signal indicates the status of the write transaction.
axi_s0_buser_o	Out	AXI_USER_WIDTH	User signals. AXI4: Optional AXI4-Lite: N/A
axi_s0_bready_i	In	1	Response ready. This signal indicates that the manager can accept a write response.
axi_s0_arvalid_i	In	1	Read address valid. This signal indicates that the channel is signaling valid read address and control information.
axi_s0_araddr_i	In	AXI_ADDR_WIDTH	Read address. The read address gives the address of the first transfer in a read burst transaction.
axi_s0_arsize_i	In	3	Burst size. This signal indicates the size of each transfer in the burst. AXI4-Lite: N/A
axi_s0_arburst_i	In	2	Burst type. The burst type and the size information determine how the address for each transfer within the burst is calculated. AXI4-Lite: N/A
axi_s0_arlen_i	In	8	AXI read burst length. This indicates the number of beats per AXI burst. AXI4-Lite: N/A
axi_s0_arid_i	In	AXI_ID_WIDTH	AXI read address ID width.
axi_s0_arlock_i	In	1	Lock type. AXI4: Optional AXI4-Lite: N/A
axi_s0_arcache_i	In	4	Memory type. AXI4: Optional AXI4-Lite: N/A
axi_s0_arprot_i	In	3	Protection type. AXI4: Optional AXI4-Lite: Optional
axi_s0_arqos_i	In	4	Quality of Service.

Pin Name	Direction	Width (Bits)	Description
			AXI4: Optional AXI4-Lite: N/A
axi_s0_arregion_i	In	4	Region. AXI4: Optional AXI4-Lite: N/A
axi_s0_aruser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional AXI4-Lite: N/A
axi_s0_arready_o	Out	1	Read address ready. This signal indicates that the subordinate is ready to accept an address and associated control signals.
axi_s0_rvalid_o	Out	1	Read valid.
axi_s0_rdata_o	Out	AXI_DATA_WIDTH	Read data.
axi_s0_ruser_o	Out	AXI_USER_WIDTH	User signals. AXI4: Optional AXI4-Lite: N/A
axi_s0_rlast_o	Out	1	Read last. This signal indicates the last transfer in a read burst.
axi_s0_rresp_o	Out	2	Read response. This signal indicates the status of the read transaction.
axi_s0_rready_i	In	1	Read ready. This signal indicates that the manager can accept the read data and response information.

2.3. Attributes Summary

Table 2.2 provides a list of user configurable attributes for this IP. The attribute values are specified upon IP generation via a Graphical User Interface.

Table 2.2. Attributes Summary

Attribute Name	Attribute ID	Selectable Values	Default	Dependency on Other Attributes
AXI4 Interface Settings				
AXI Data Bus Width	AXI_DATA_WIDTH	8,16,32,64,128, 256	32	—
AXI Address Width	AXI_ADDR_WIDTH	2-32	12	—
AXI ID Width	AXI_ID_WIDTH	1-8	4	—
AXI USER Width	AXI_USER_WIDTH	1-128	4	—
AXI Interface Type	AXI_INTERFACE_TYPE	AXI4, AXI4-LITE	AXI4	—
AXI4 Register Settings				
Number of AXI Registers	REG_COUNT	4-1024	4	—
AXI Subordinate Base Address	REG_ADDR_RANGE_BASE	—	0000	—
AXI Subordinate End Address	REG_ADDR_RANGE_END	—	0FFF	—

Table 2.3. Attributes Description

Attribute Name	Description
AXI4 Interface Settings	
AXI Data Bus Width	Specifies the bit width of AXI data bus and AXI registers data bus.

Attribute Name	Description
AXI Address Width	Specifies the bit width of AXI address signals.
AXI ID Width	Specifies the bit width of AXI ID signals.
AXI USER Width	Specifies the bit width of AXI USER signals.
AXI Interface Type	Specifies the specific AXI4 Protocol used.
AXI4 Register Settings	
Number of AXI Registers	Specifies the number of AXI Registers to be generated by the module.
AXI Subordinate Base Address	Specifies the base address for this AXI Subordinate in hex format.
AXI Subordinate End Address	Specifies the base address for this AXI Subordinate in hex format.

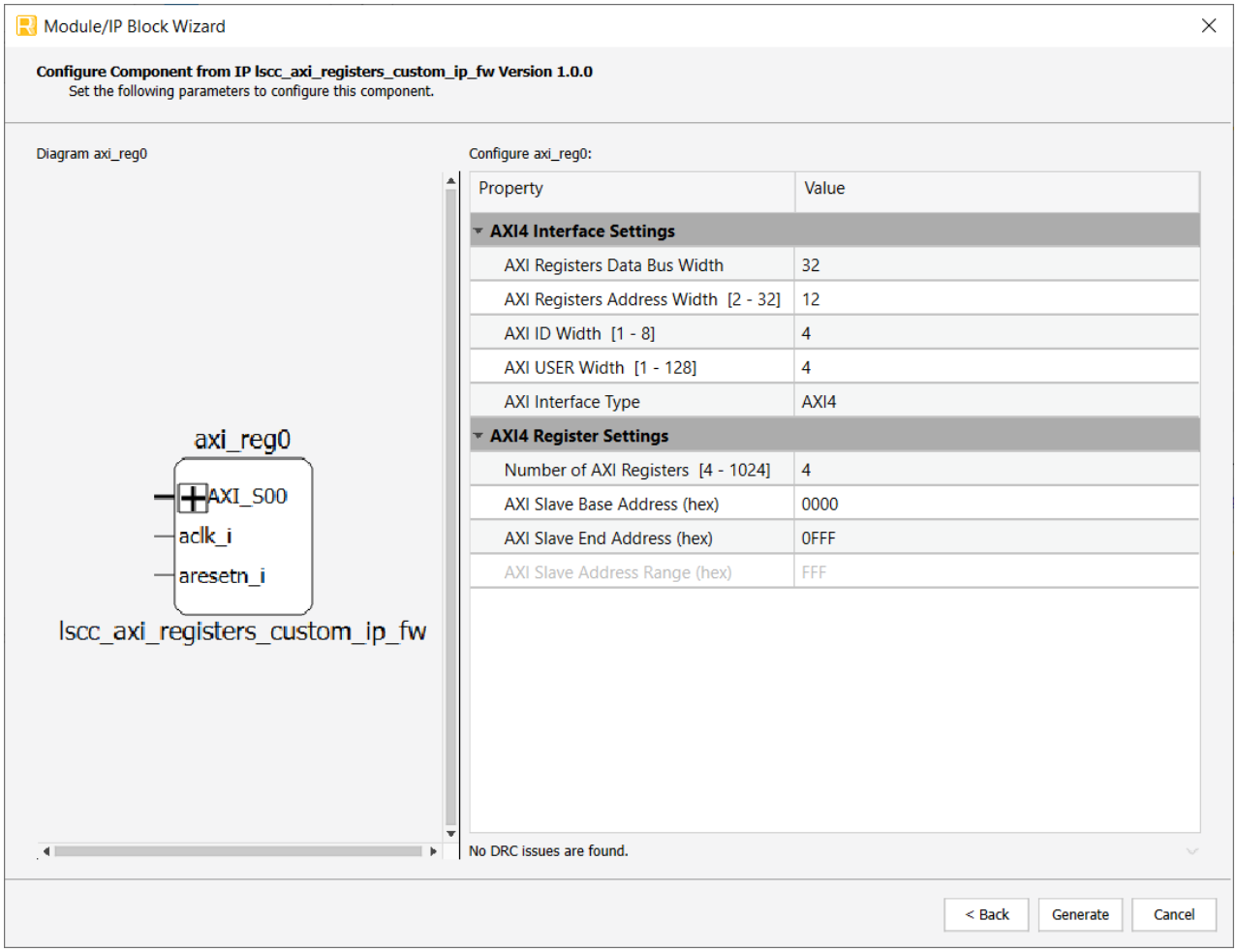

Figure 2.2. IP Generation GUI

2.4. Error Responses

The following are implemented response behaviors for some transaction settings.

- EXOKAY and DECERR responses are unused.

Only SLVERR response is currently implemented. EXOKAY is not implemented since exclusive access using AWLOCK and ARLOCK is unused.

- Transaction to a non-existing AXI4 register address has SLVERR response.

If the register address being accessed with either a single or burst transaction exceeds the expected addresses (which is REG_COUNT x number of byte lanes for AXI4, or just REG_COUNT for AXI4-Lite), the error response returns SLVERR. On additional note, all Write and Read transactions on addresses before the error should be successful.

- AXI4 FIXED and WRAP burst is responded with SLVERR response.

The only supported burst transaction is INCR since it is the suitable behavior for sequential memory implementation.

- If the resulting data bytes by AWSIZE/ARSIZE is larger than AXI_DATA_WIDTH, the size that is used by default is the maximum data width, but also triggers a SLVERR response.

This behavior flags the user that the intended data bytes is not suitable to the configured data width.

Appendix A. Resource Utilization

Table A.1 shows device and tool used to collect the resource utilization data of this IP. Table A.2 and Table A.3 show the resource utilization of AXI Registers for Custom IP Framework with AXI4 Interface and AXI4-Lite Interface, respectively.

Table A.1. Device and Tool Tested

	Value
Lattice Radiant Software Version	Radiant Software 2022.1 (for Windows)
Device Used	LAV-AT-500E-2LFG1156I
Synthesis Tool	Synplify Pro (R) S-2021.09LR-1-Beta, Build 268R, Mar 24 2022

Table A.2. Resource Utilization for AXI4 Interface

AXI_DATA_WIDTH	AXI_ADDR_WIDTH	REG_COUNT	Fmax (MHz)	Register	LUT	EBR
8	32	8	251.762	168	334	0
8	32	32	251.762	264	423	0
8	32	256	230.947	1160	1120	0
16	32	8	251.762	273	529	0
16	32	32	251.762	689	859	0
16	32	256	215.796	4258	3512	0
32	32	8	251.762	418	690	0
32	32	32	250.752	1189	1338	0
32	32	256	177.462	8364	6986	0
64	32	8	251.762	707	1000	0
64	32	32	234.357	2277	2294	0
64	32	256	158.856	16601	13658	0
128	32	8	221.631	1323	2037	0
128	32	32	208.247	4366	4443	0
128	32	256	150.807	33121	274545	0
256	32	8	168.180	2466	3544	0
256	32	32	195.351	8604	9597	0
256	32	128	114.929	33233	30170	0

Table A.3. Resource Utilization for AXI4-Lite Interface

AXI_DATA_WIDTH	AXI_ADDR_WIDTH	REG_COUNT	Fmax (MHz)	Register	LUT	EBR
32	32	8	250.00	283	400	0
32	32	32	250.00	1051	1003	0
32	32	256	176.554	8220	6442	0
64	32	8	250.00	539	653	0
64	32	32	239.808	2075	1737	0
64	32	256	166.861	16411	13261	0

References

AMBA AXI4 Protocol Specification.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, November 2022

Section	Change Summary
All	Production release.

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