

Avant Versa Board

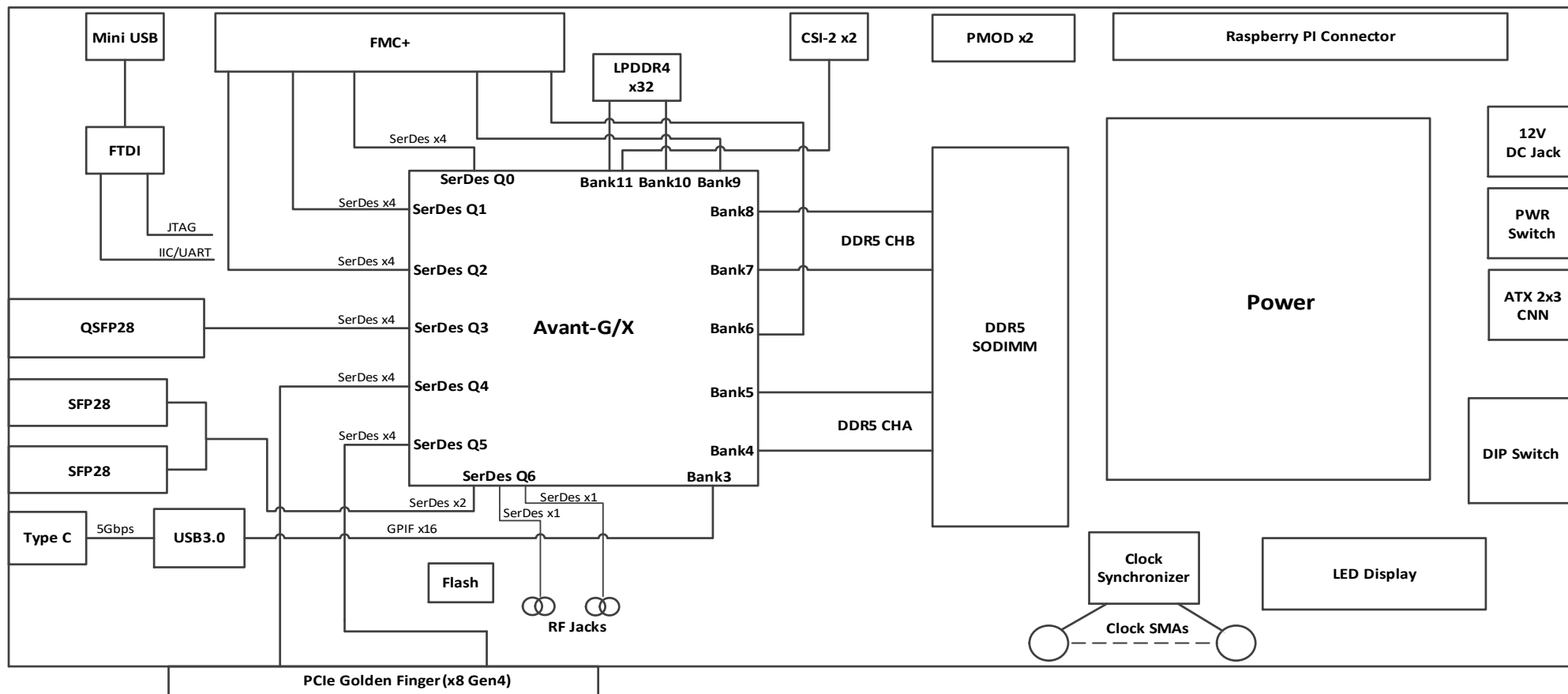
Rev - B

- | | |
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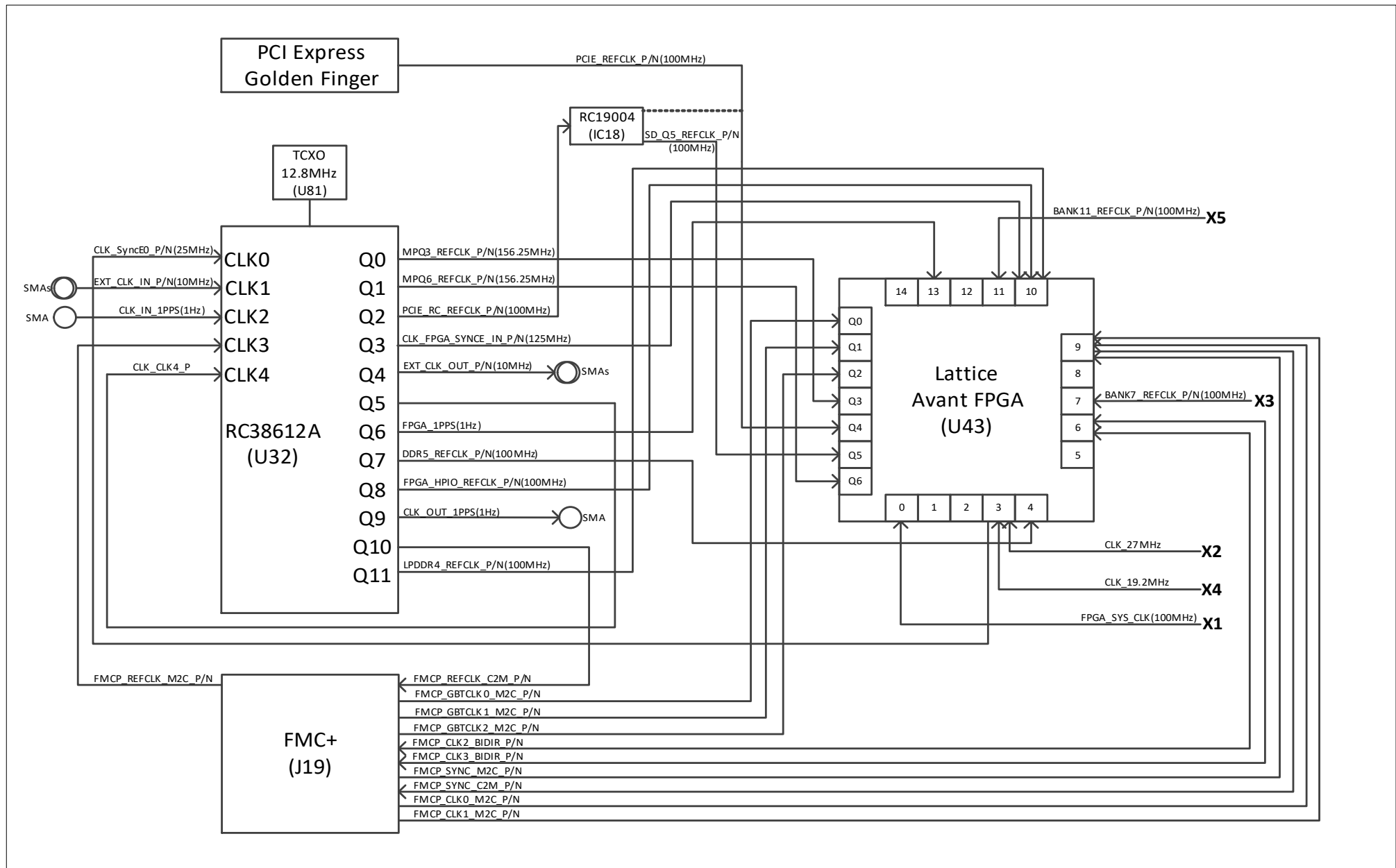
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Title			
Title			
Size	Project	Schematic Rev 1.0	
B	Avant Versa Board	Board Rev	B
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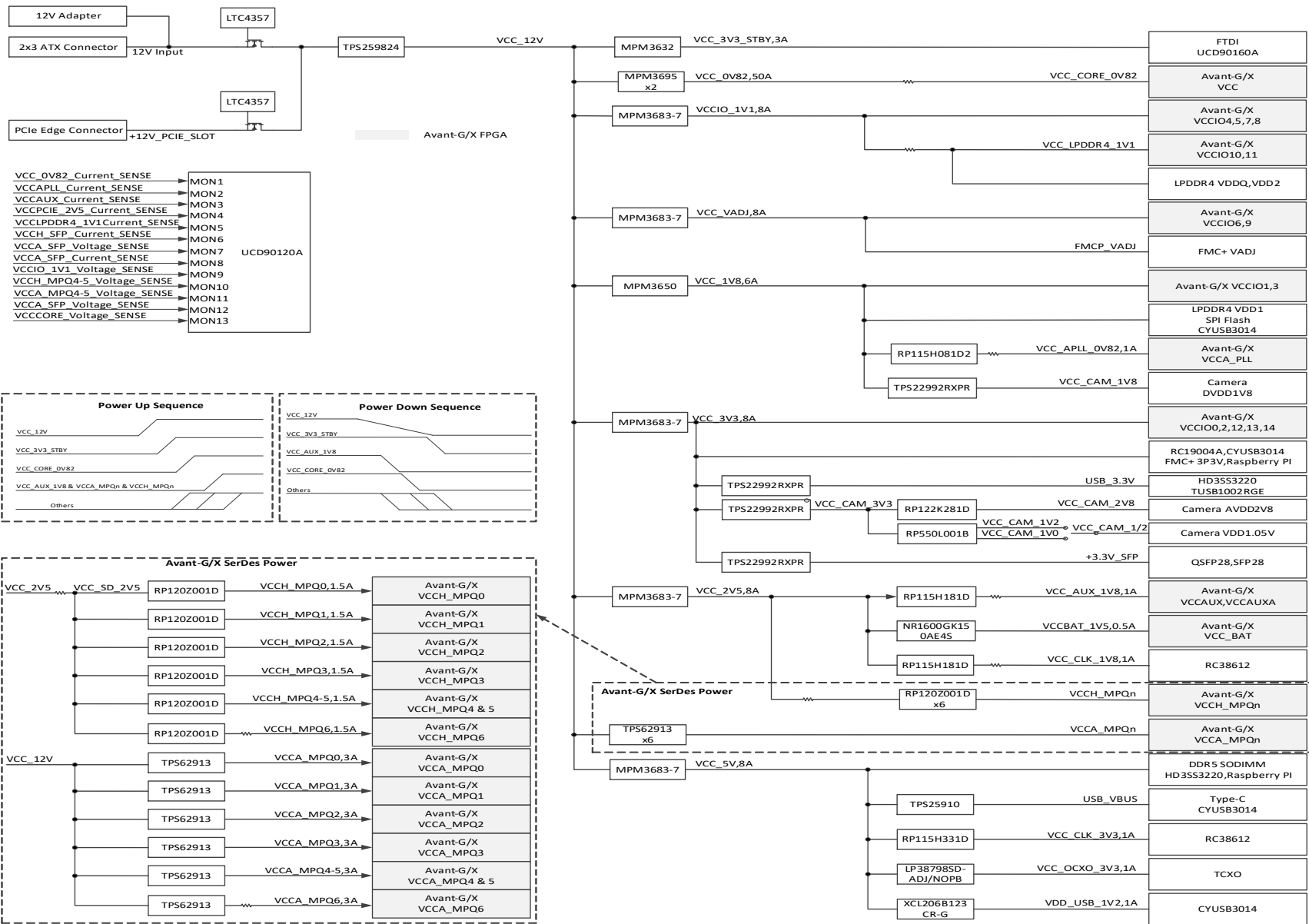
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Title Block_Diagram			
Size B	Project Avant Versa Board	Schematic Rev 1.0 Board Rev B	
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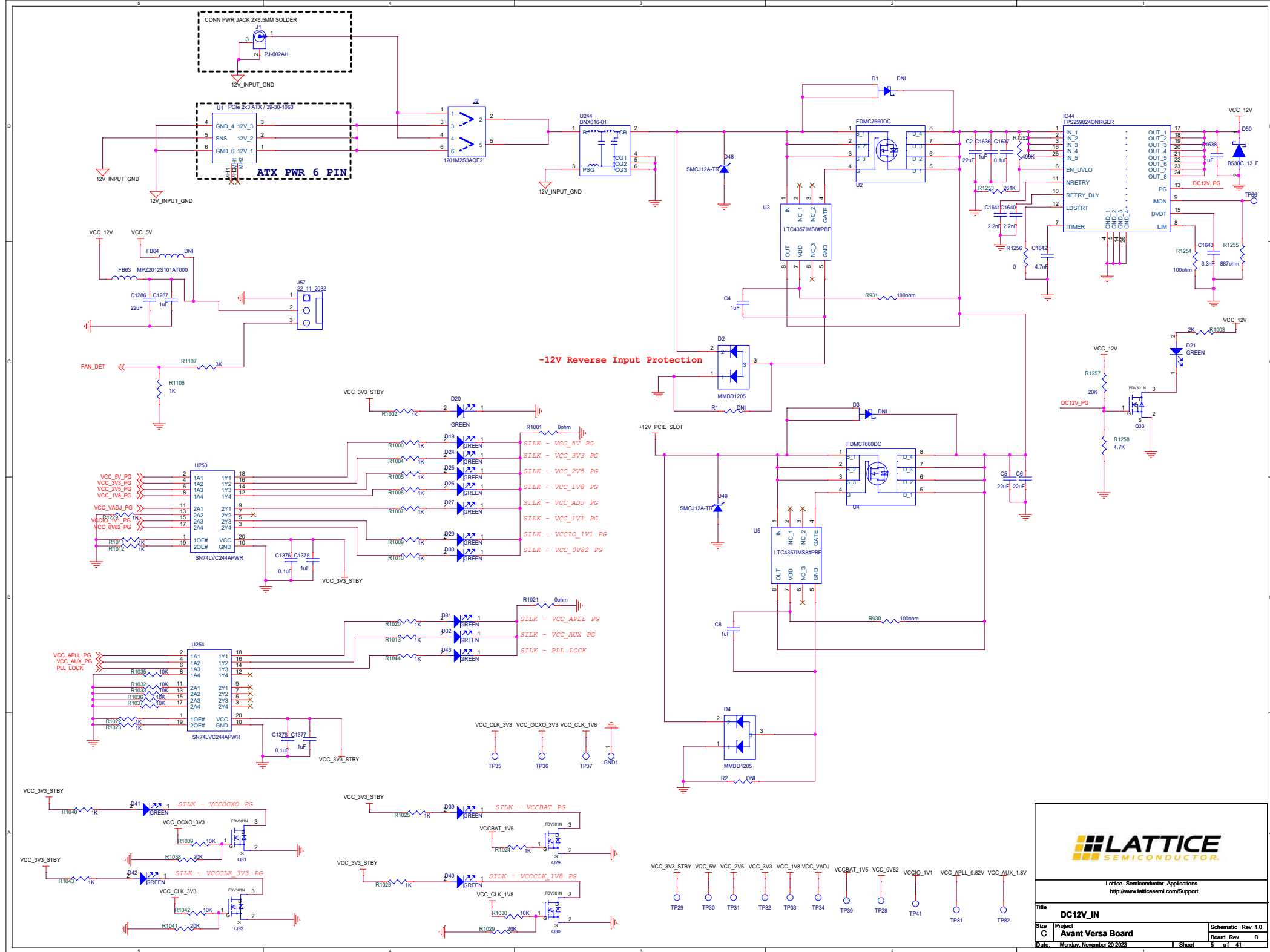


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Title		
Clock_Diagram		
Size	Project	Schematic Rev 1.0
C	Avant Versa Board	Board Rev B
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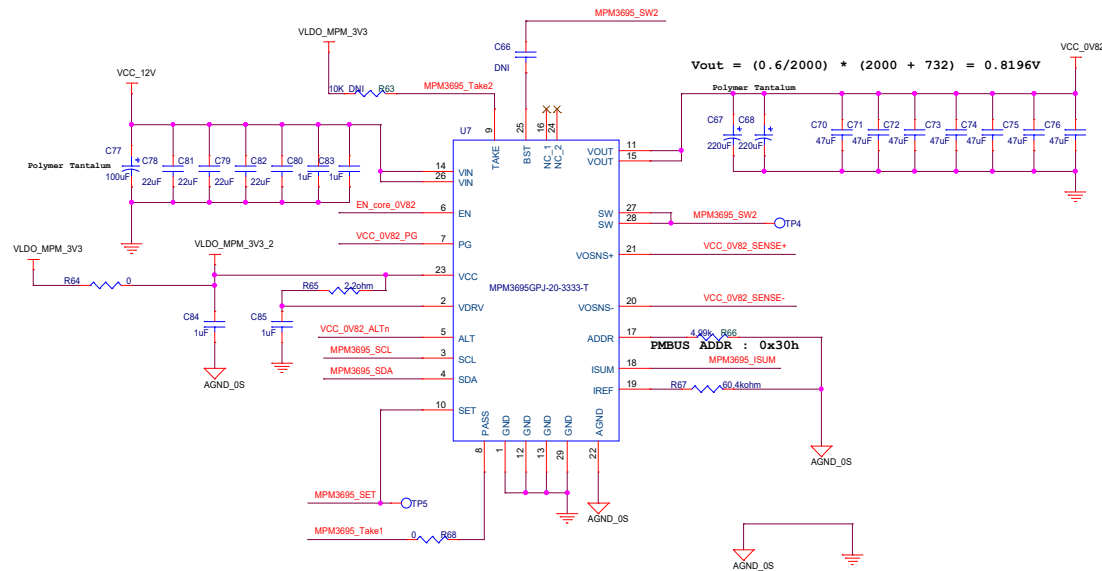
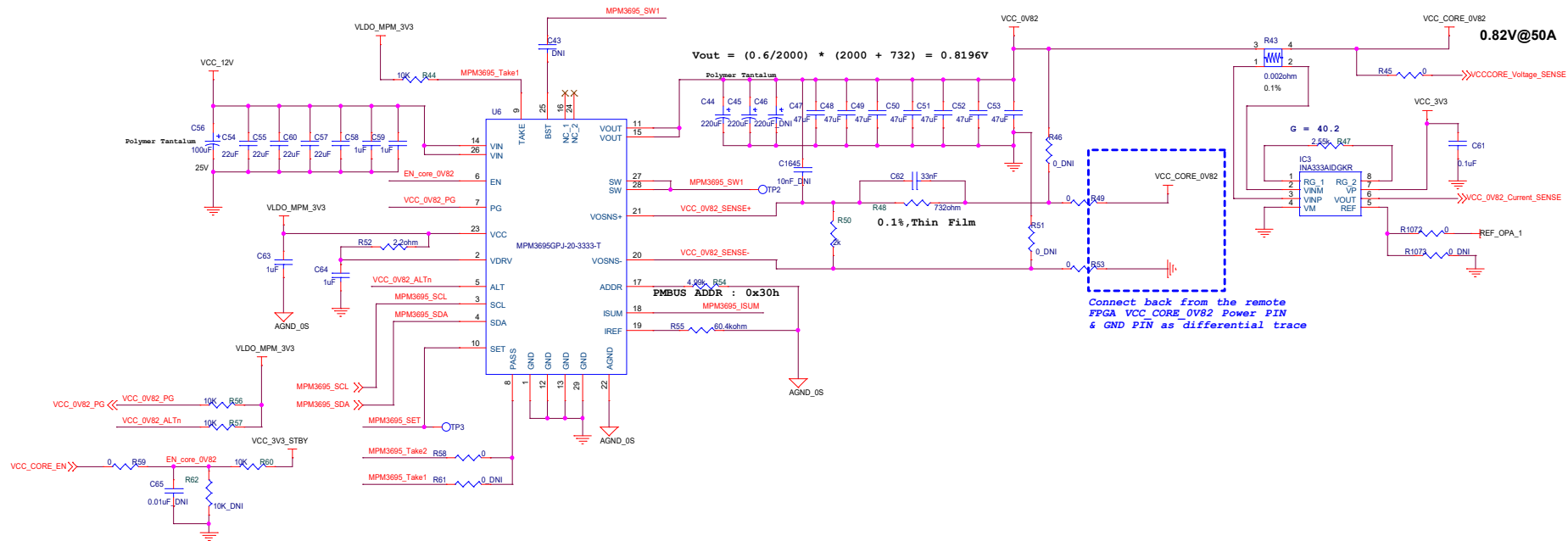


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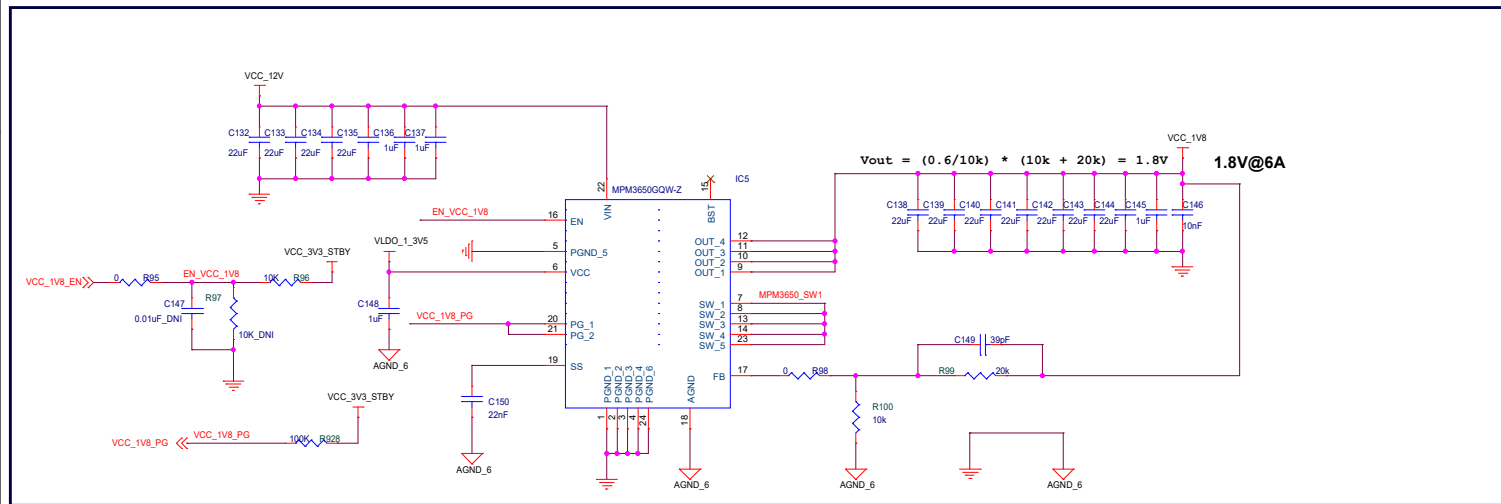
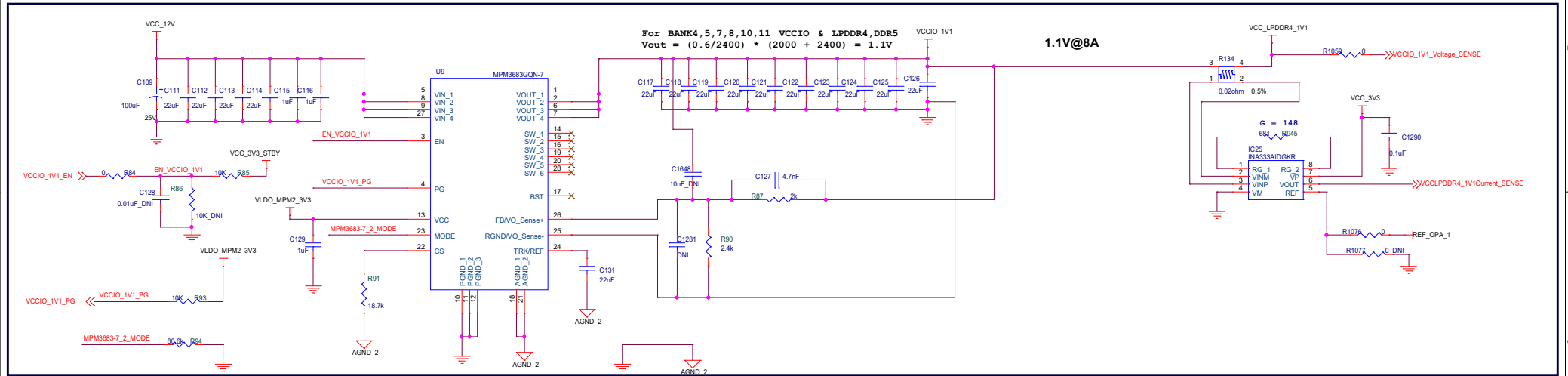
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Size	Project	Schematic Rev 1.0	
C	Avant Versa Board	Board Rev B	
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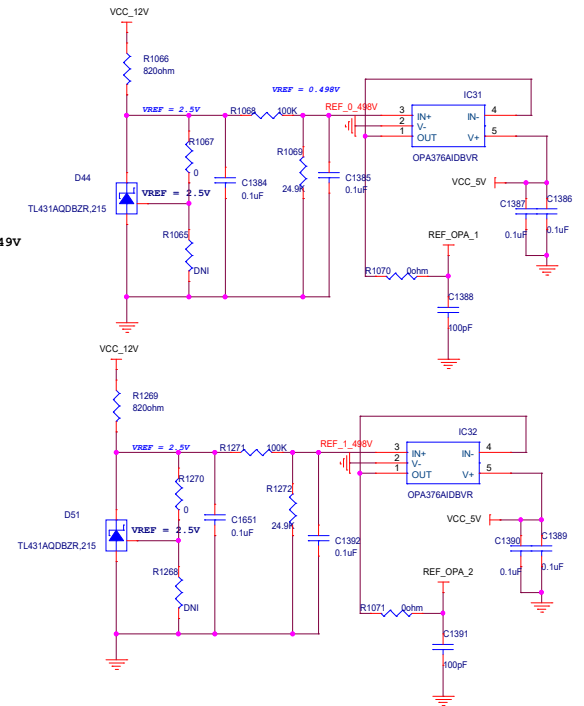
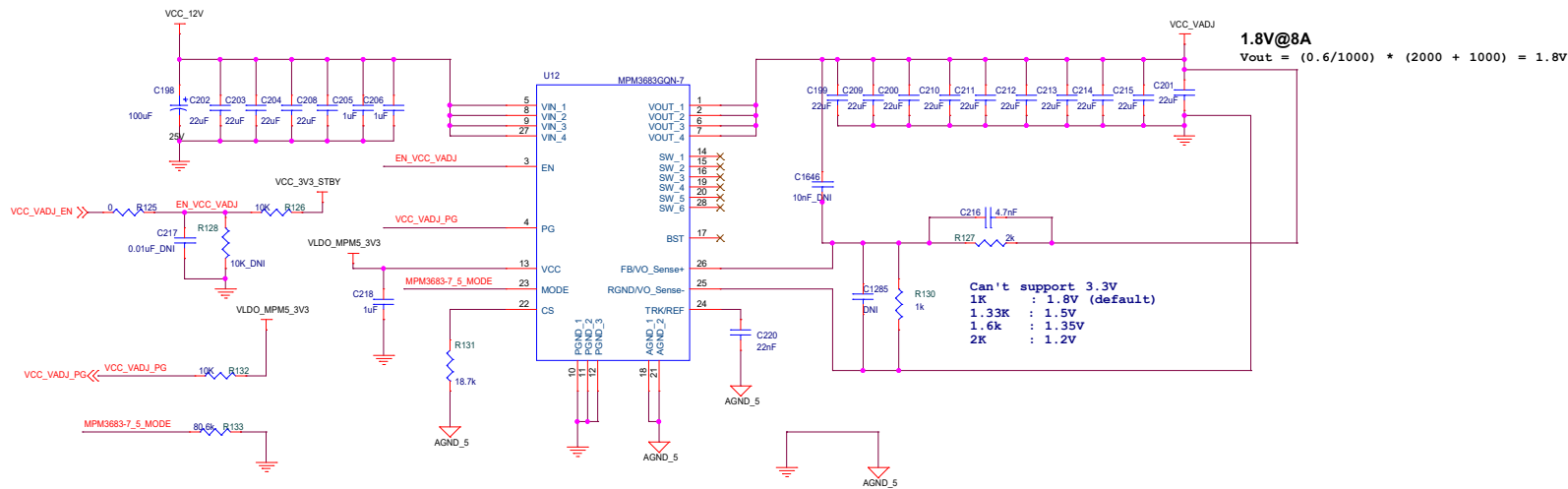
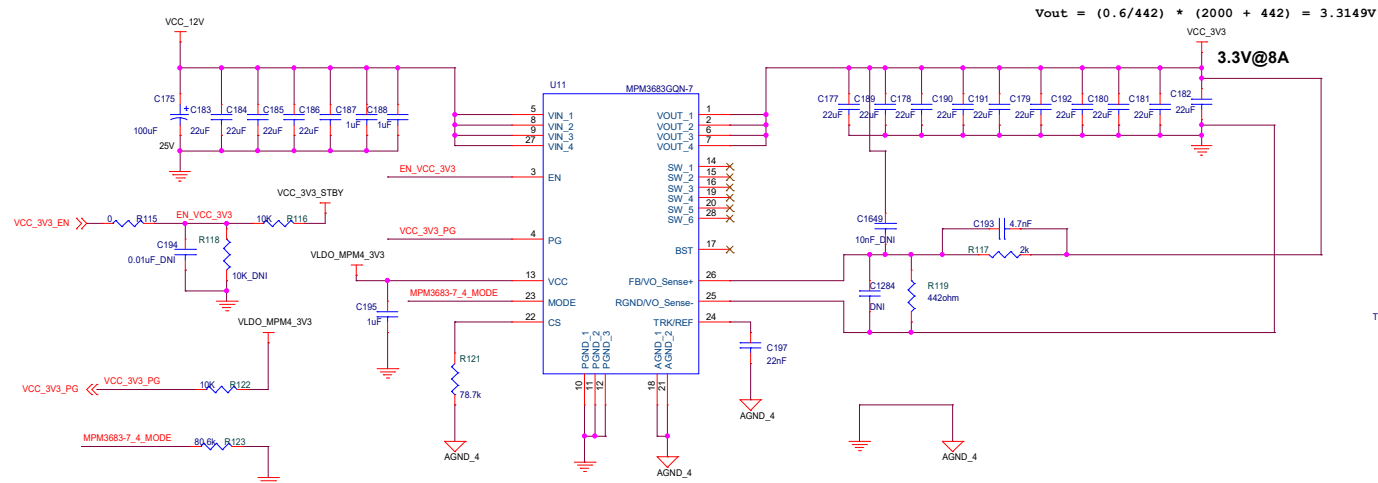
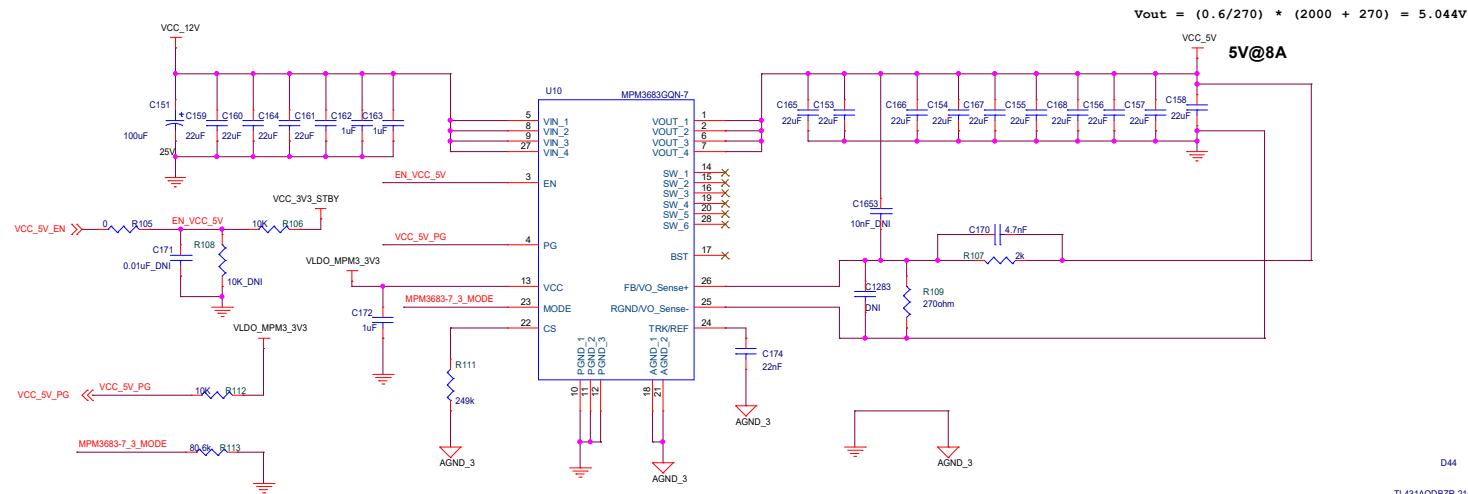
Lattice Semiconductor Applications
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Title DC/DC_VCC		
Size C	Project Avant Versa Board	Schematic Rev 1.0
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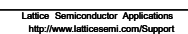
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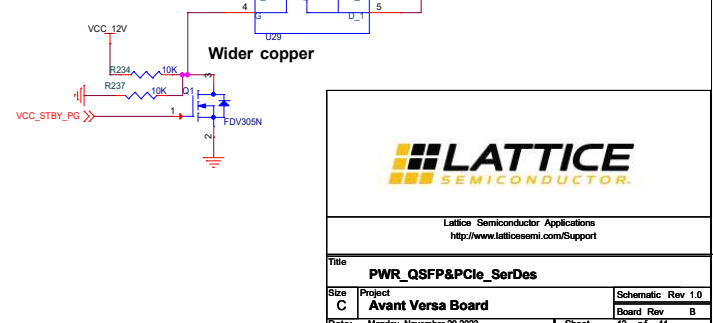
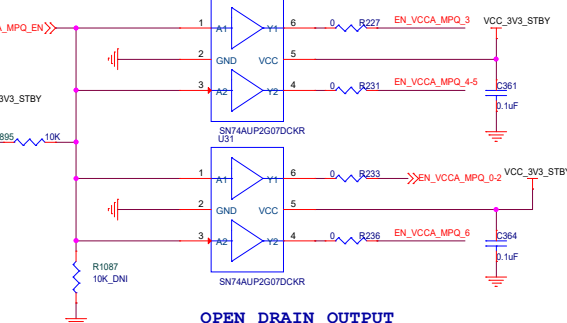
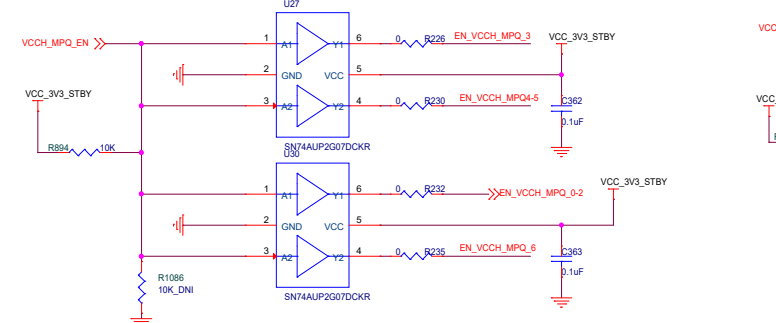
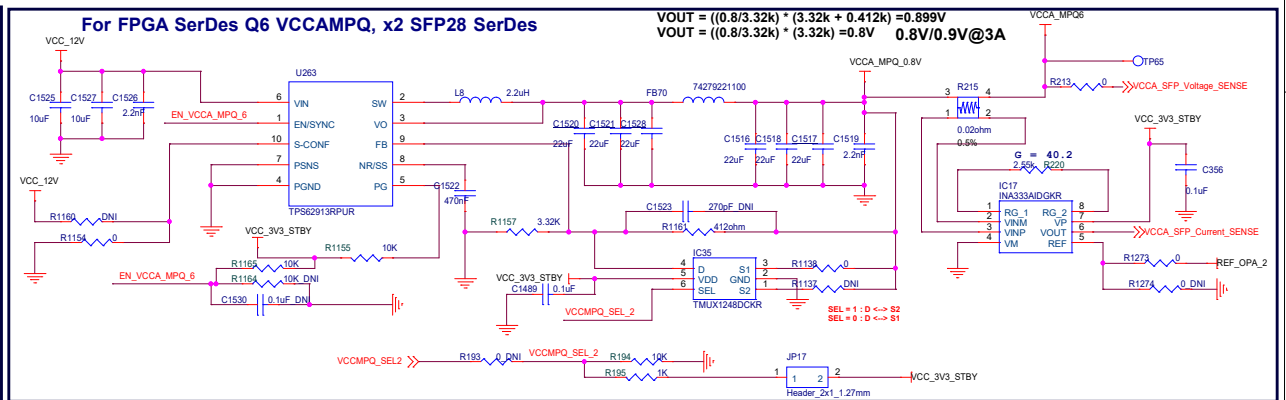
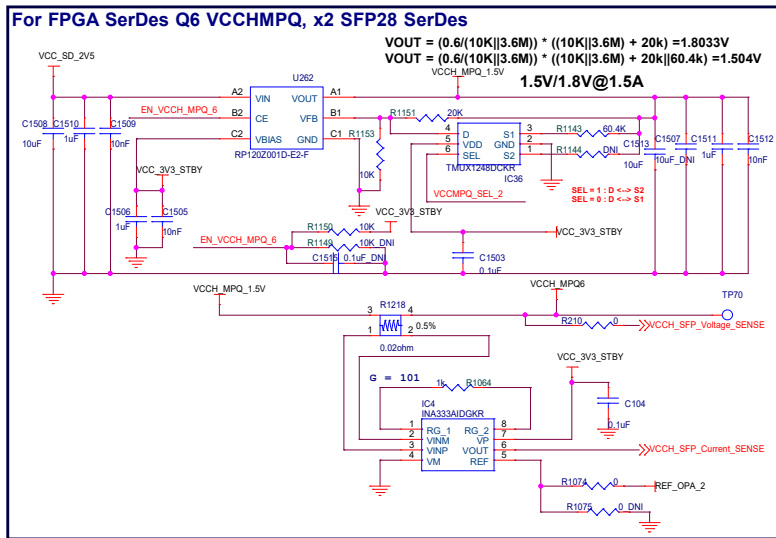
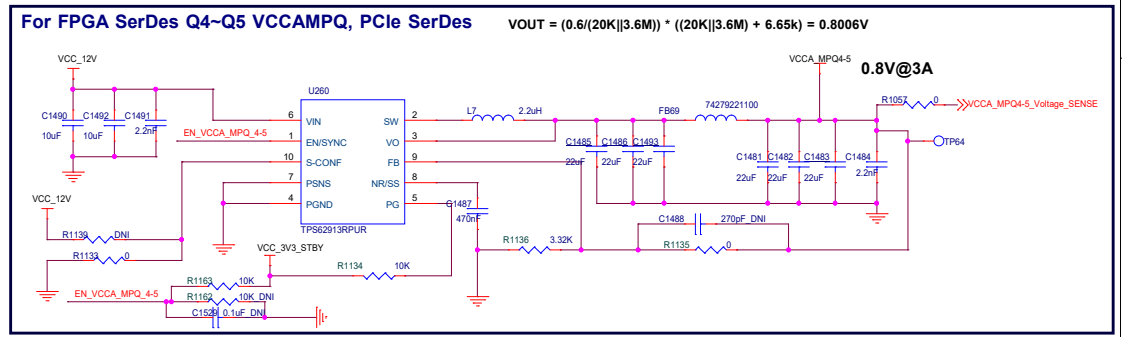
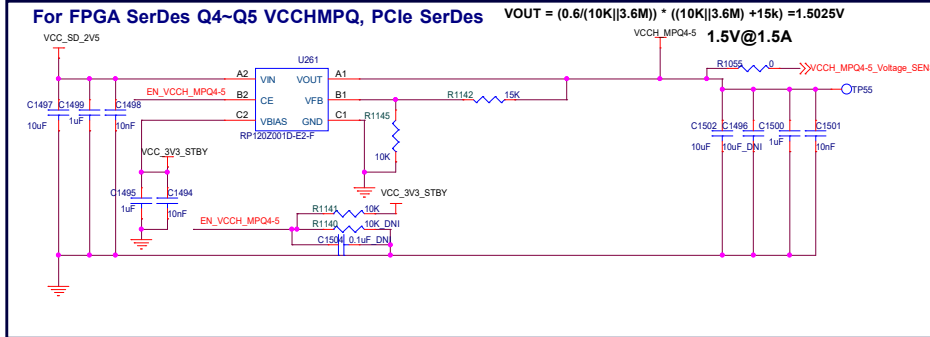
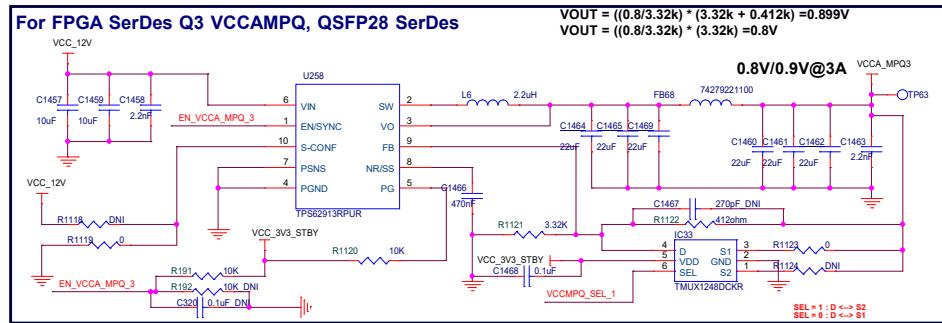
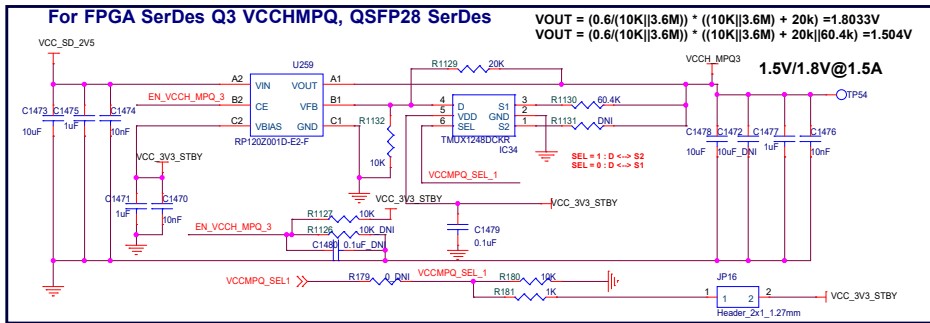
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Size	Project	Schematic Rev 1.0
C	Avant Versa Board	Board Rev B
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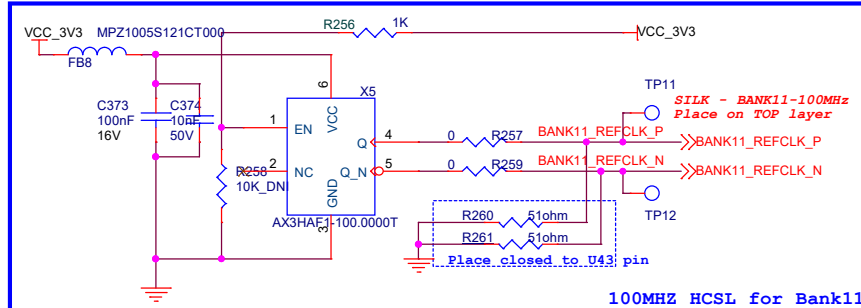
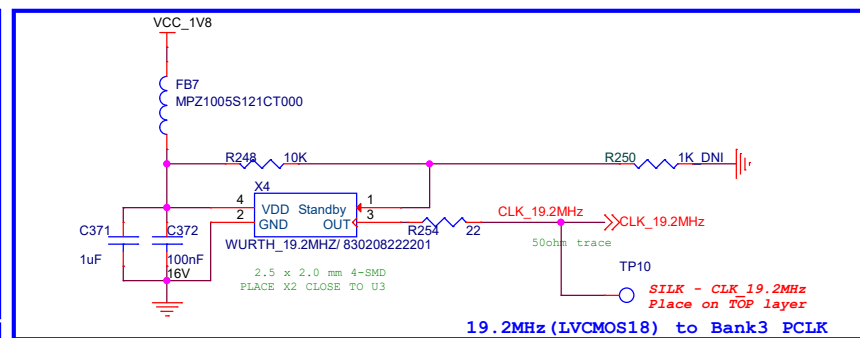
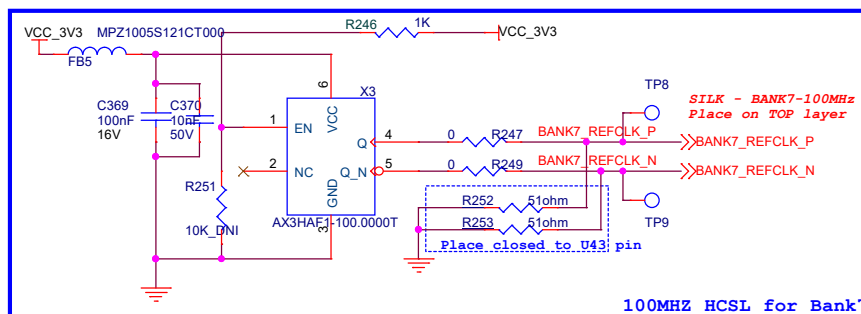
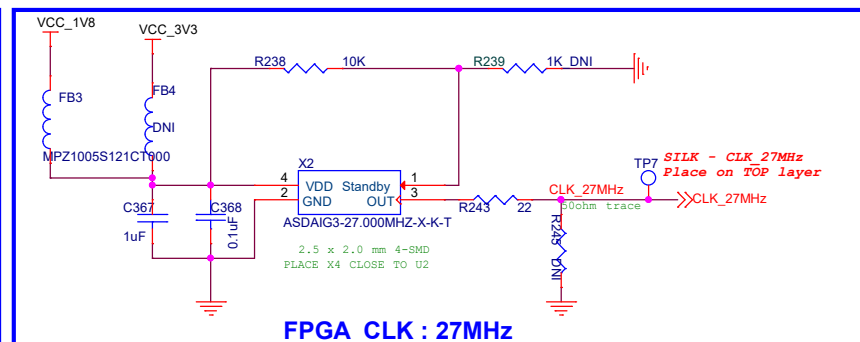
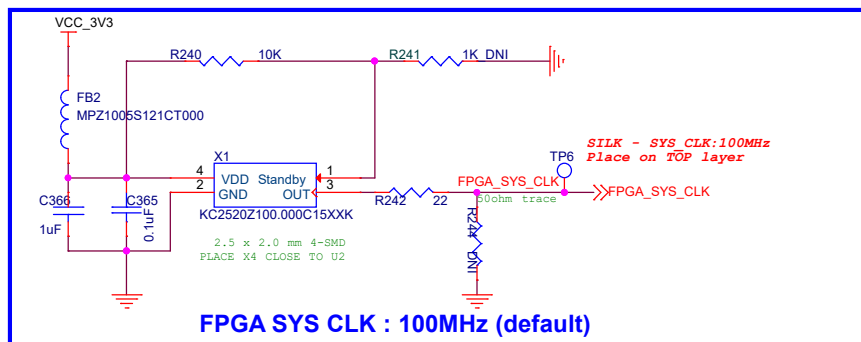


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Title			DC/DC_3
Size	Project	Schematic Rev 1.0	
C	Avant Versa Board	Board Rev B	
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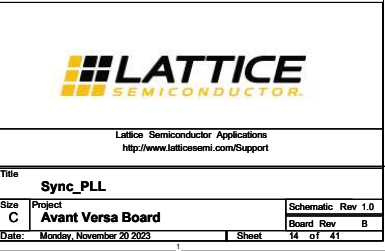


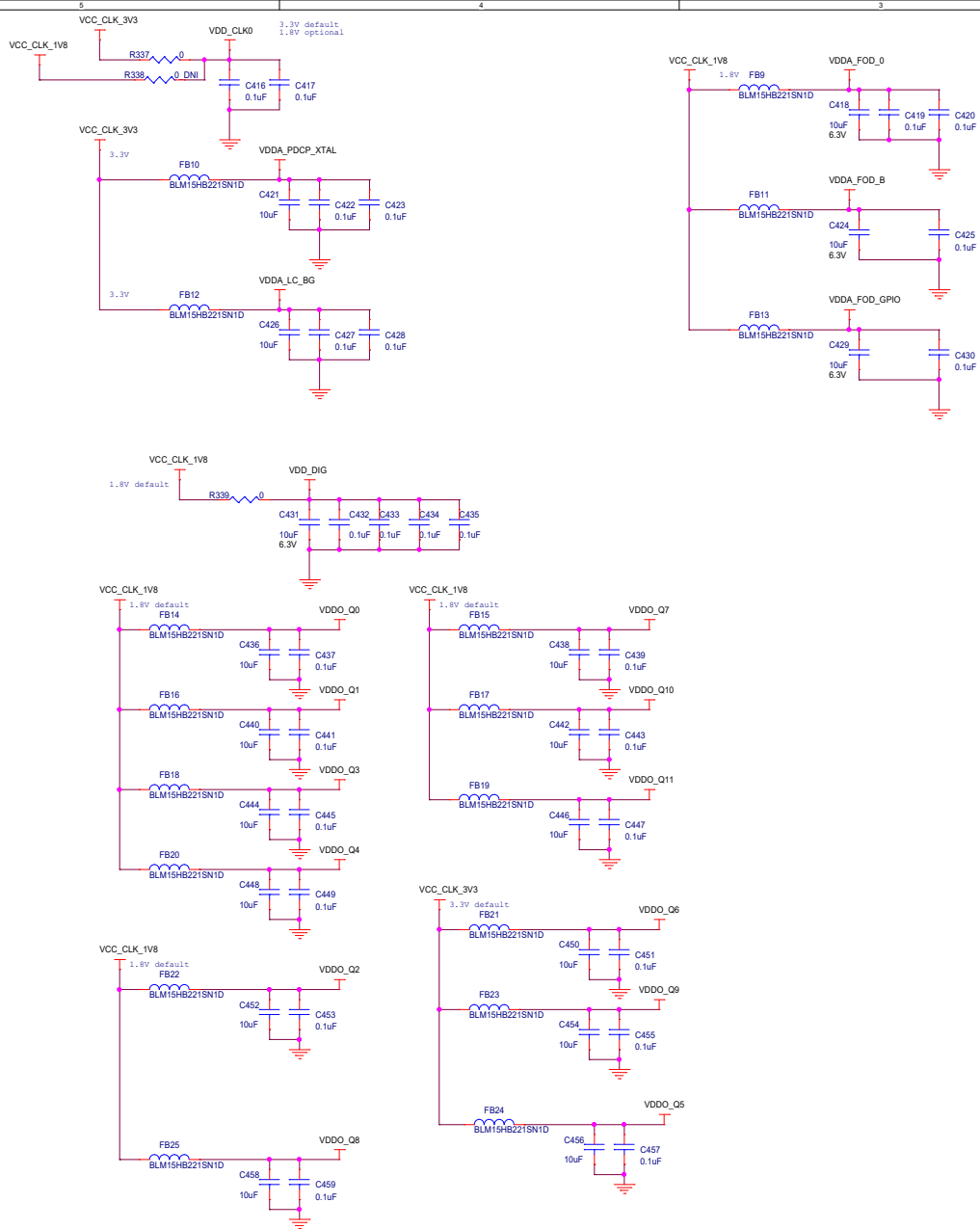




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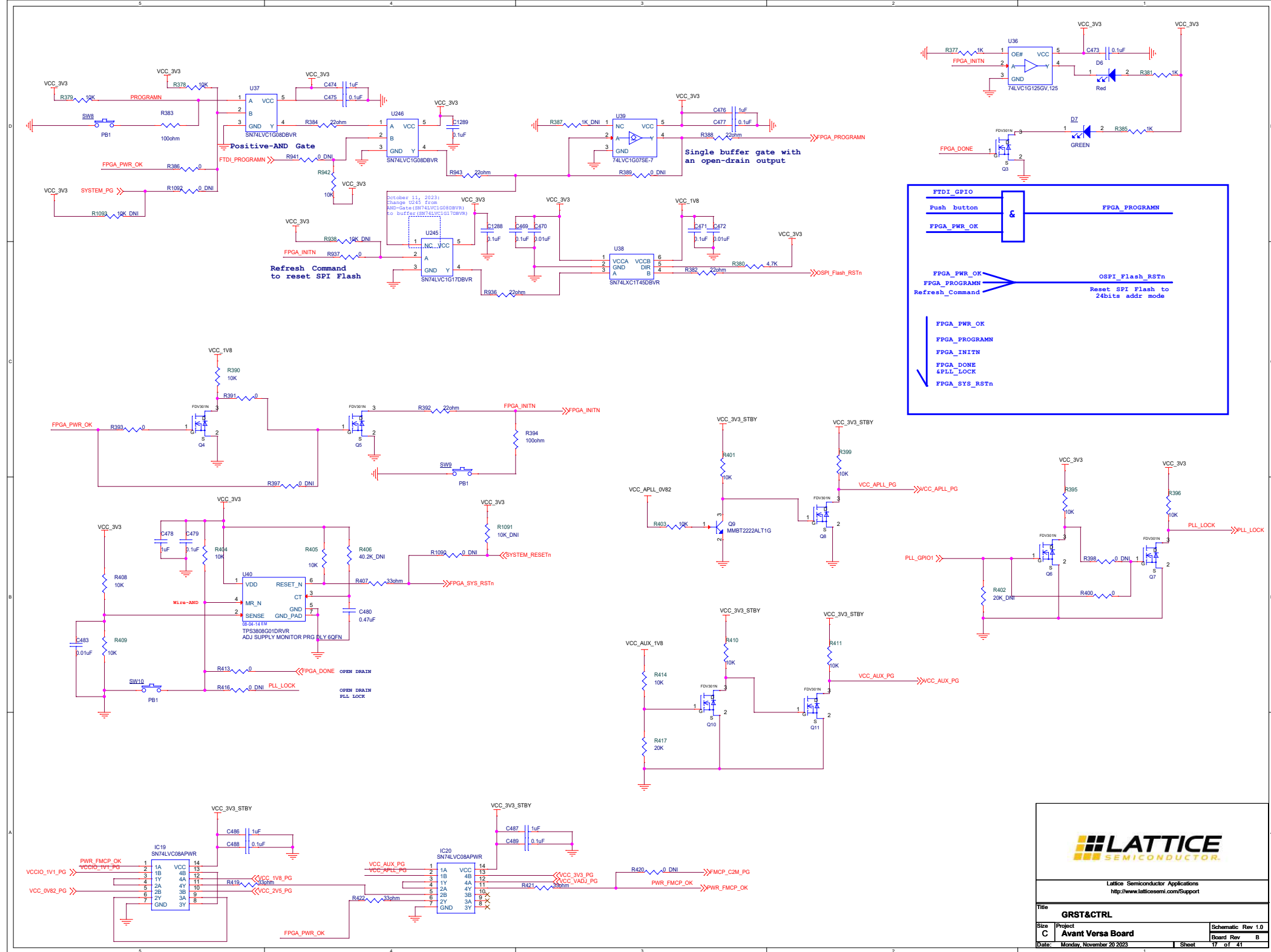
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Size B	Project Avant Versa Board	Schematic Rev 1.0
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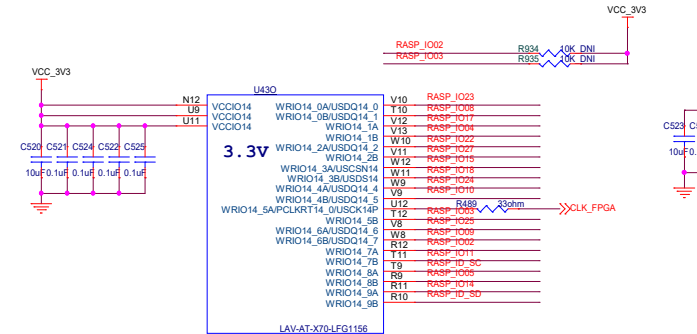
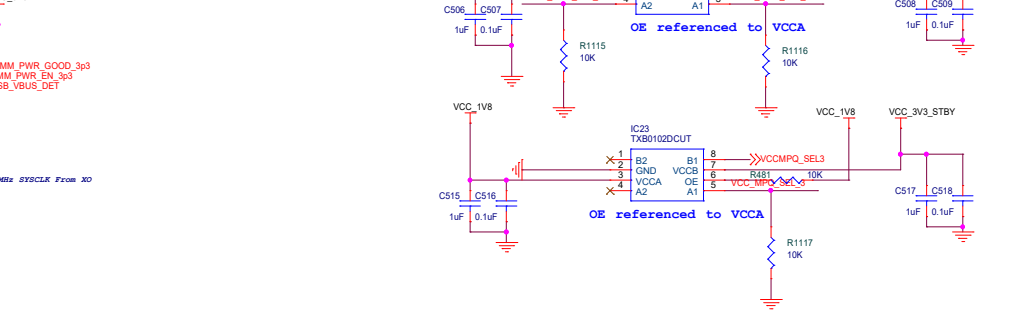
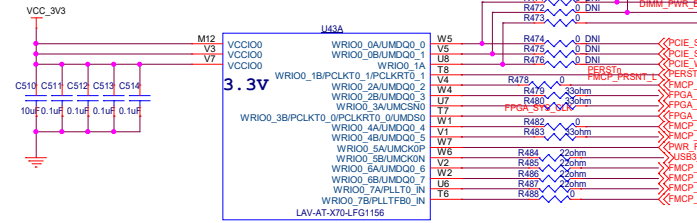
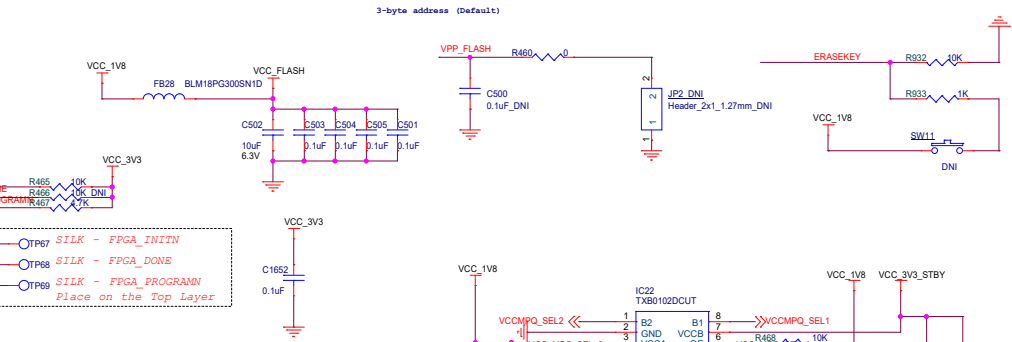
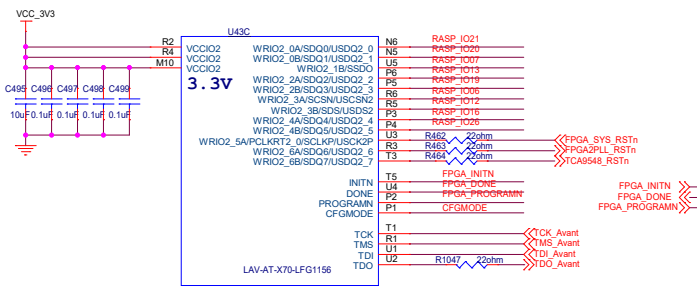
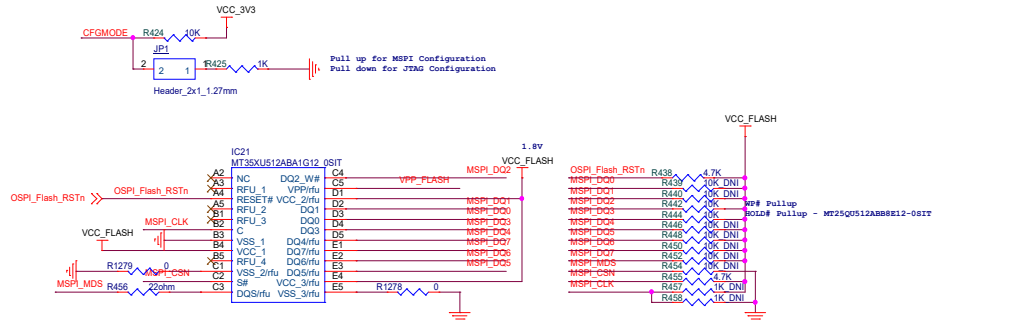
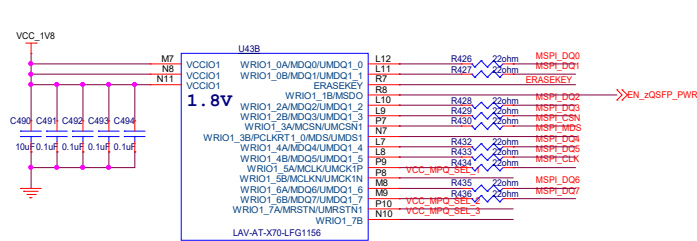


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Title		
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Size	Project	Schematic Rev 1.0
C	Avant Versa Board	Board Rev B
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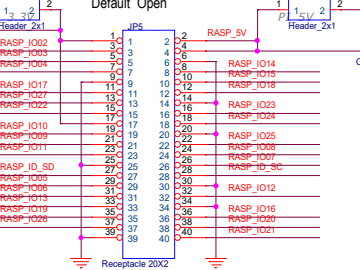


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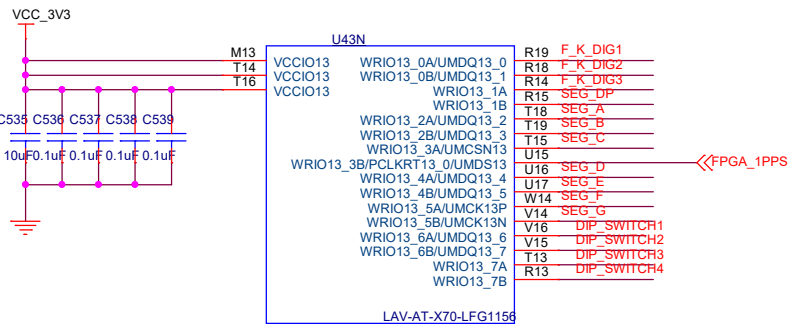
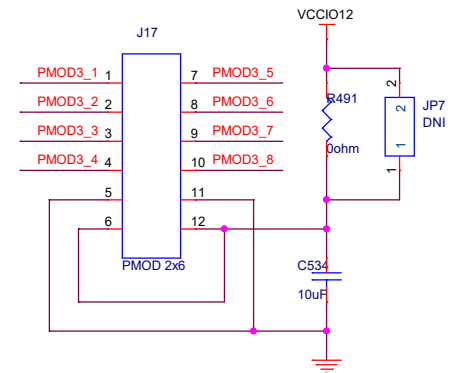
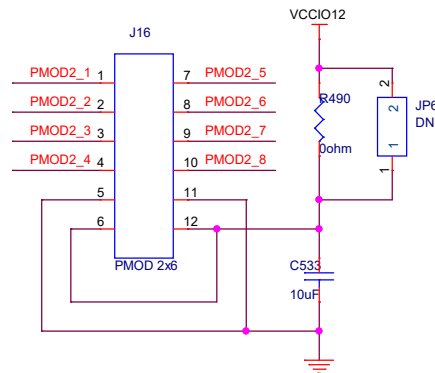
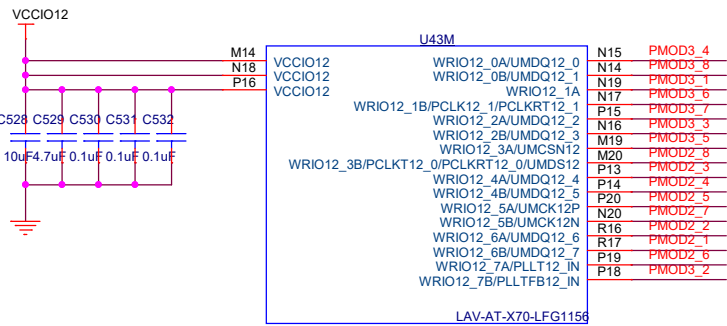
Raspberry PI and User I/O Connector

JP3 & JP4 Power For JP5
Default Open

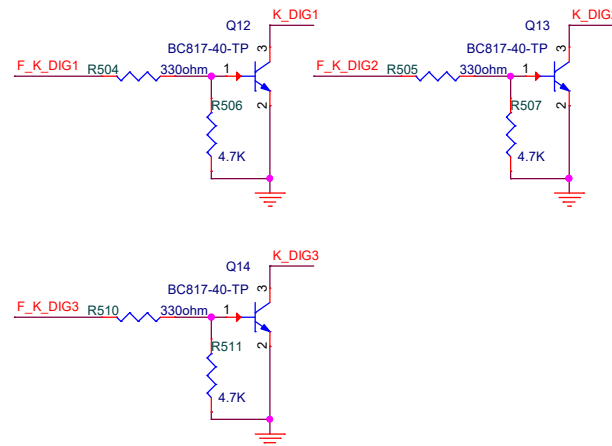
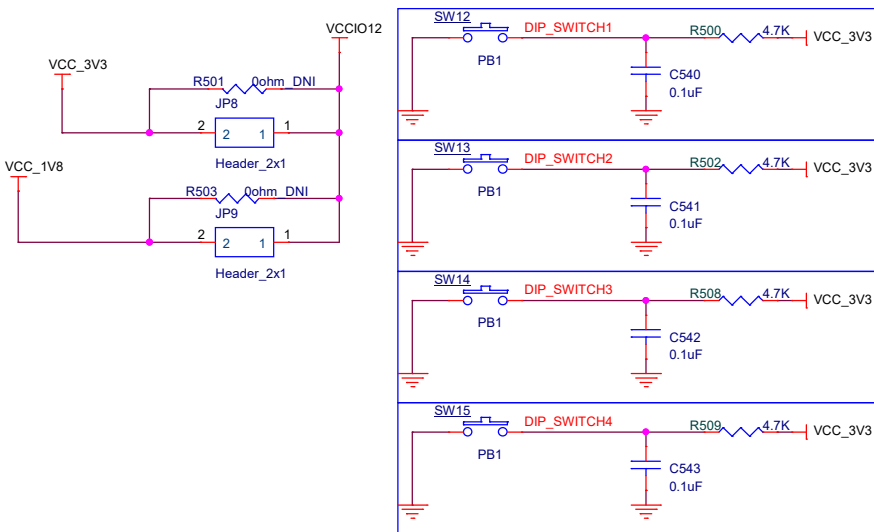
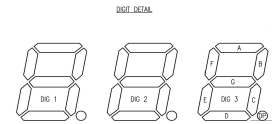


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Title FPGA_CFG&Raspberry_IO		
Size C	Project Avant Versa Board	Schematic Rev 1.0
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7_SEGMENT_DISPLAY_SECTION



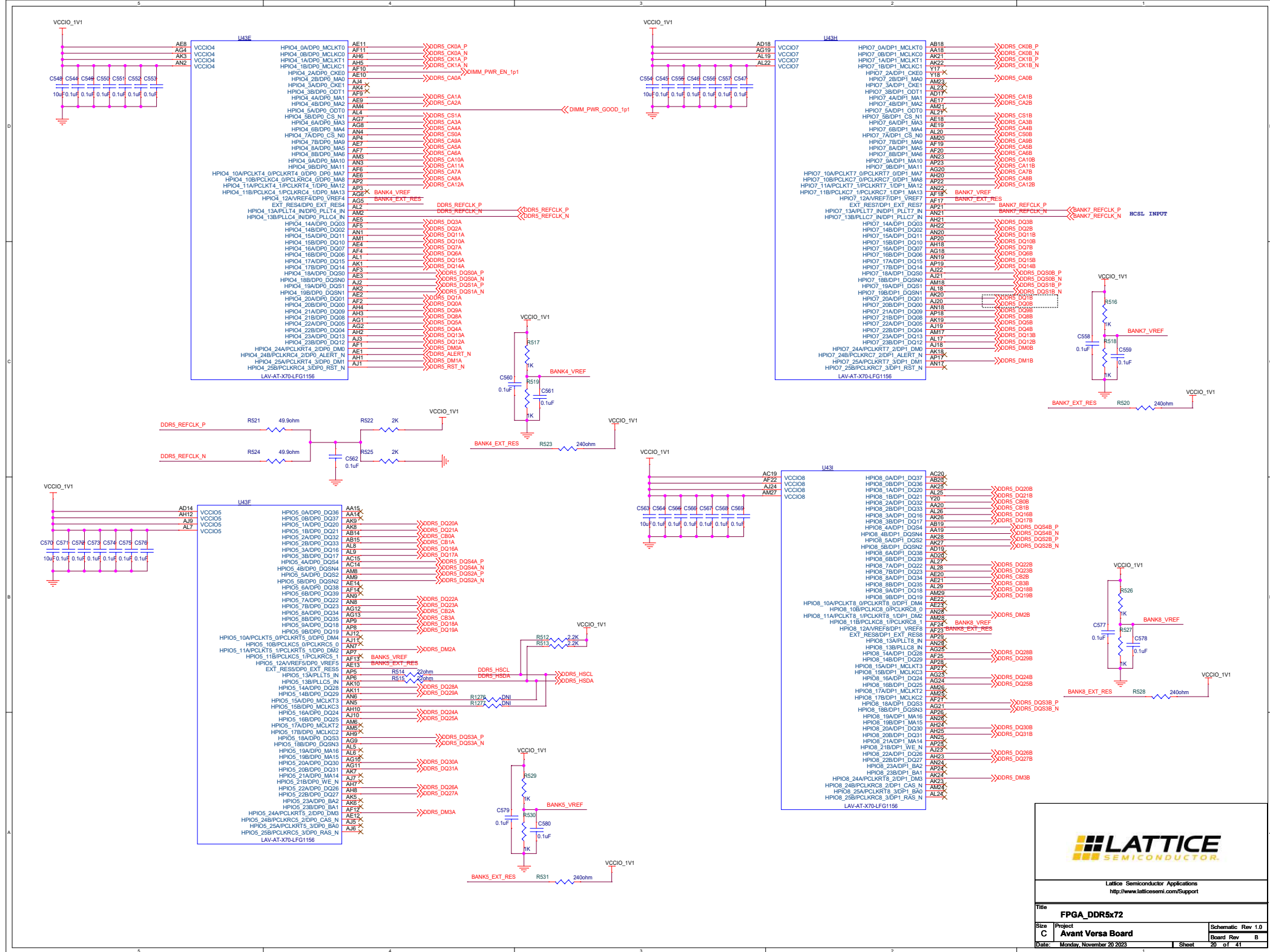
Character Signal Map

U43 PIN	D8 PIN	SEGMENT
R15	3	DP
V14	5	G
W14	10	F
U17	1	E
U16	2	D
T15	4	C
T19	7	B
T18	11	A

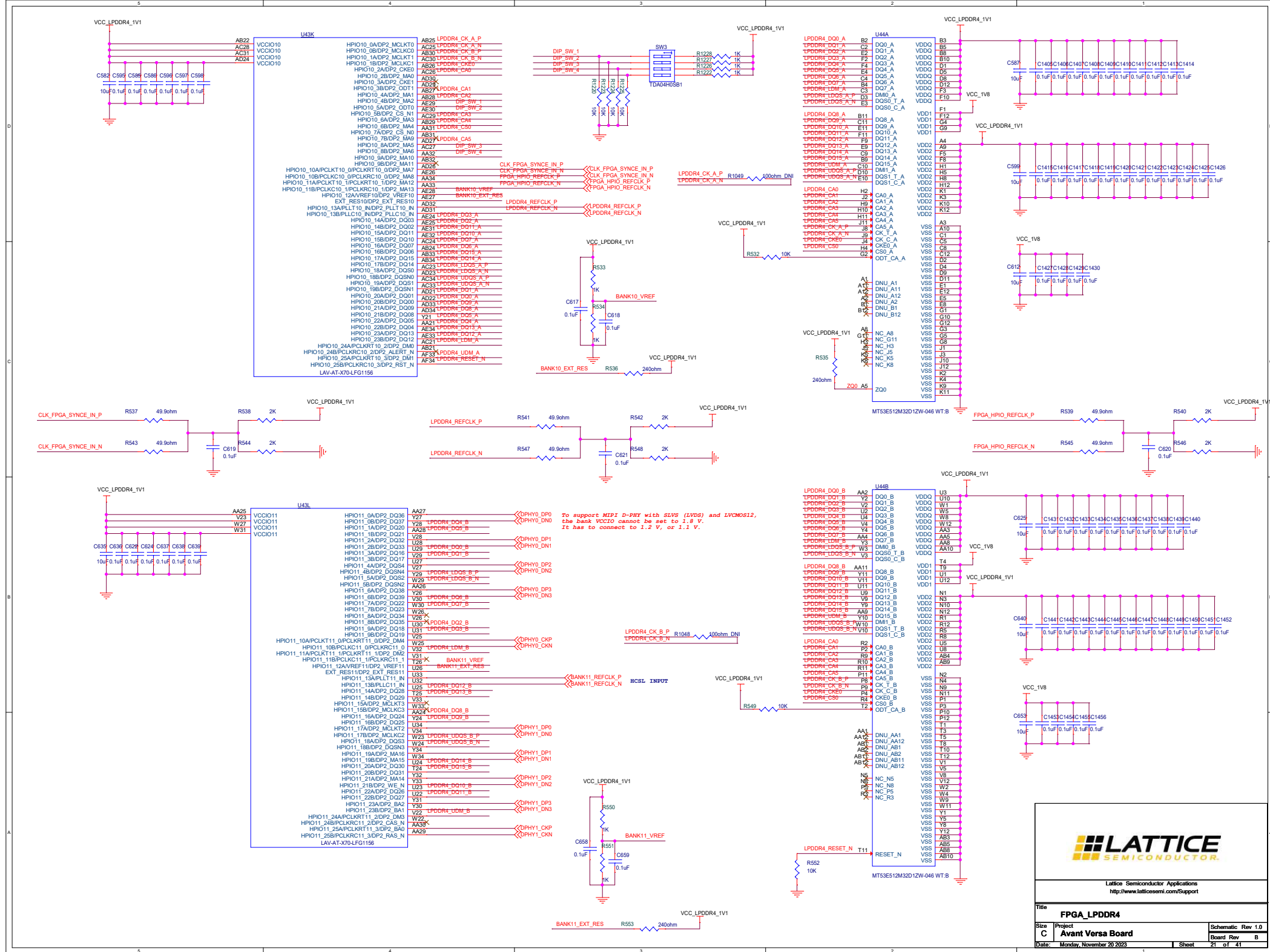



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Title FPGA_PMODE&Display		
Size B	Project Avant Versa Board	Schematic Rev 1.0
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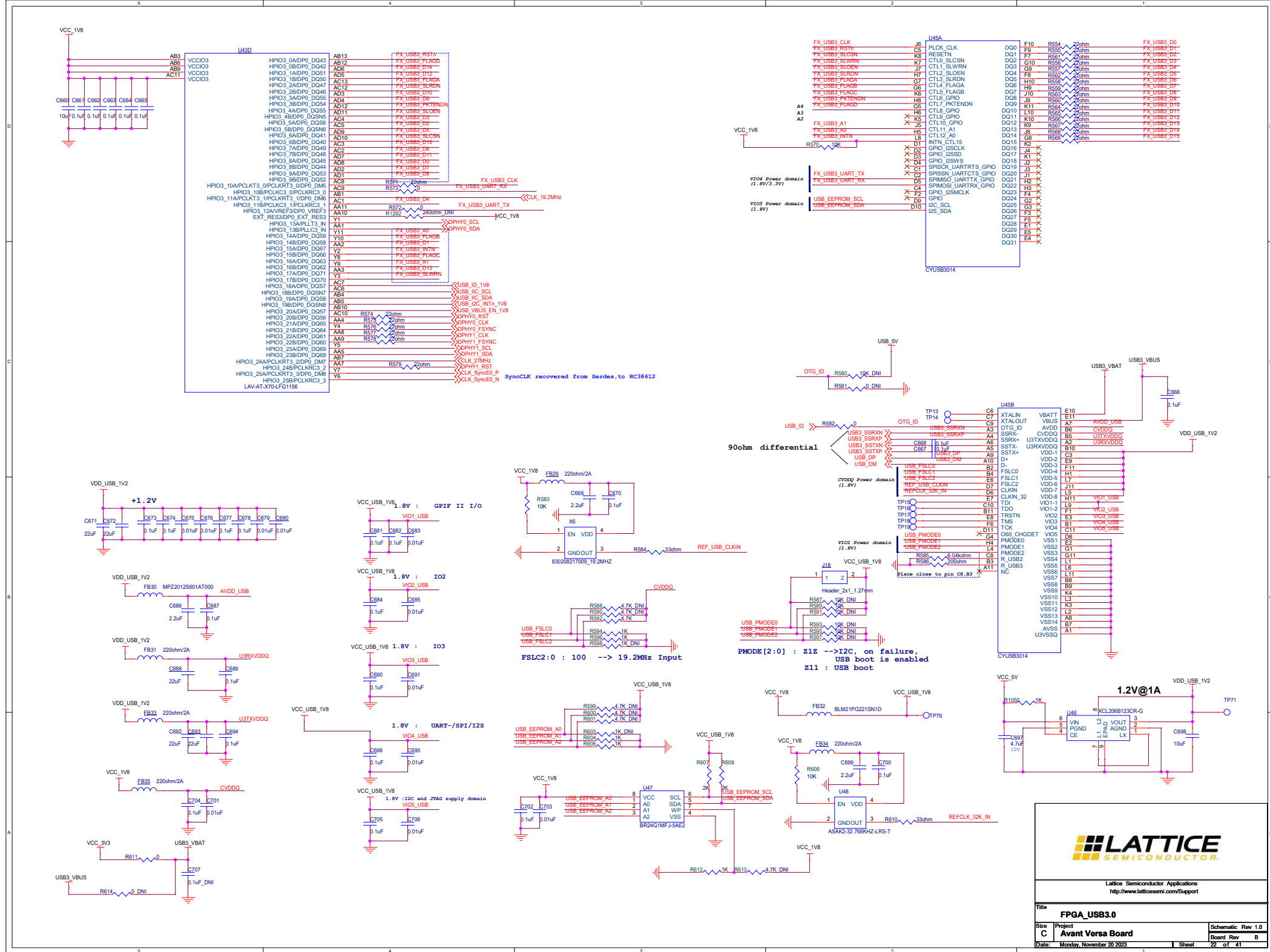
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<http://www.latticesemi.com/Support>





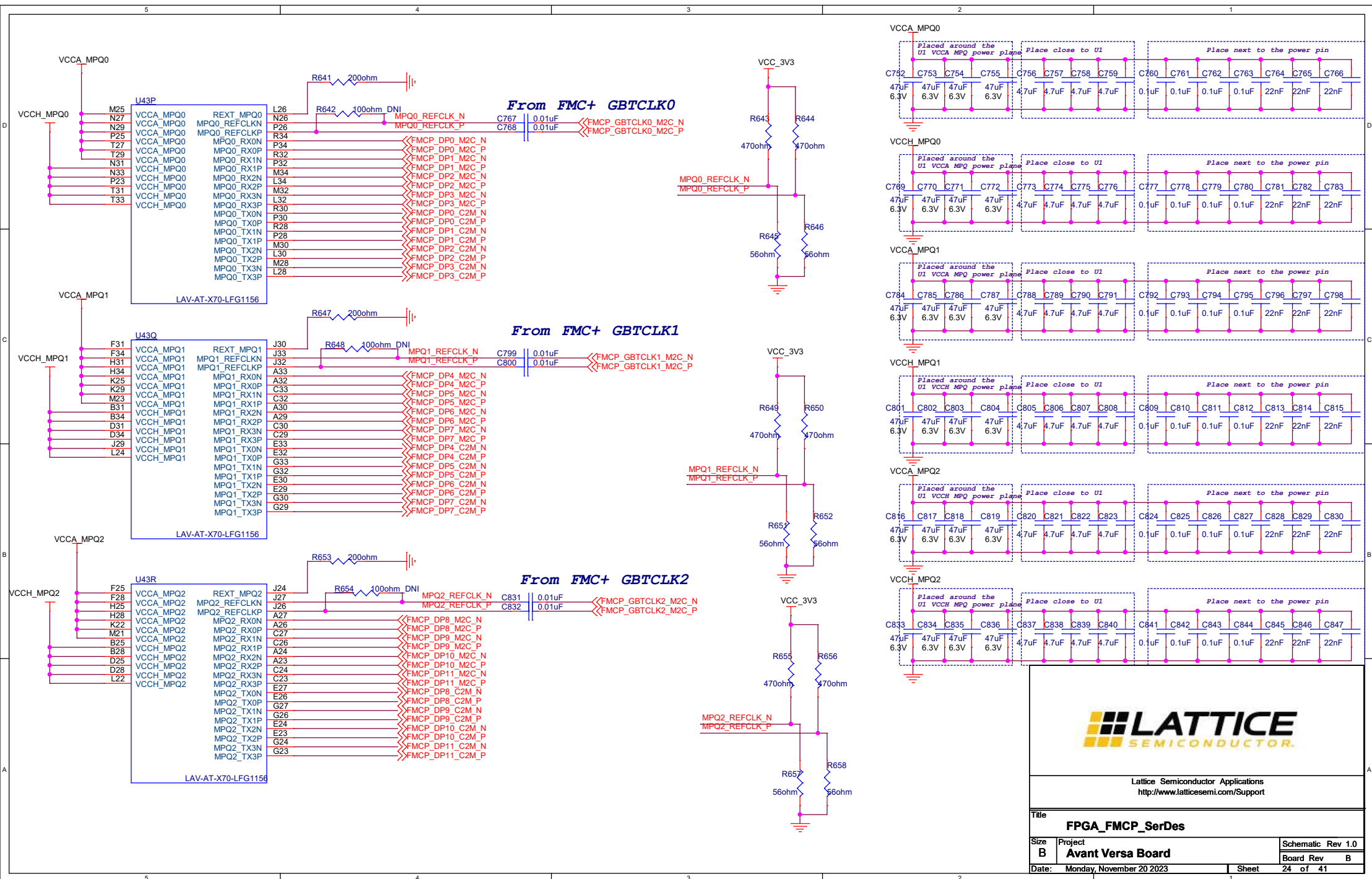
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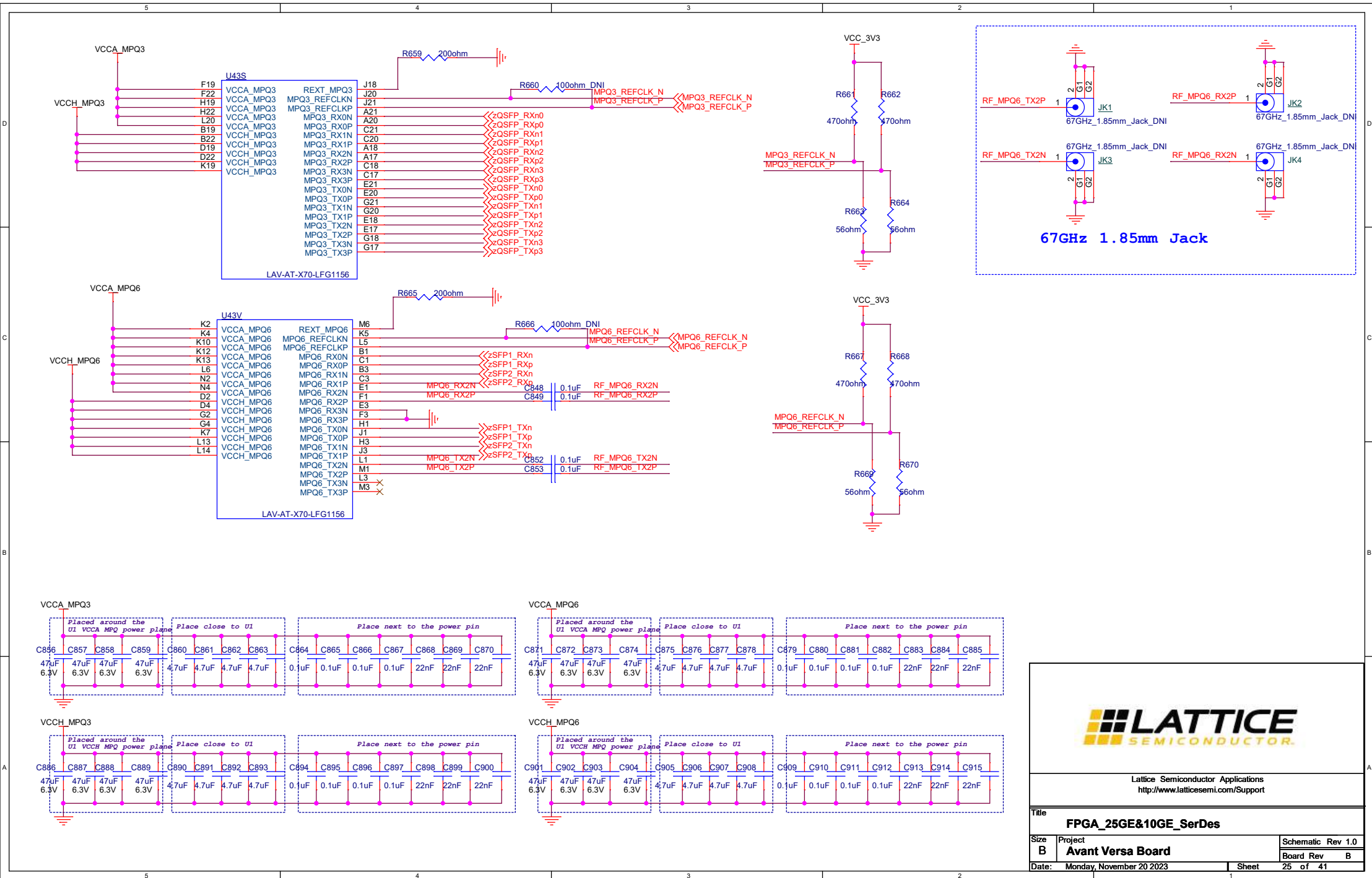
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Size C	Project Avant Versa Board	Schematic Rev 1.0
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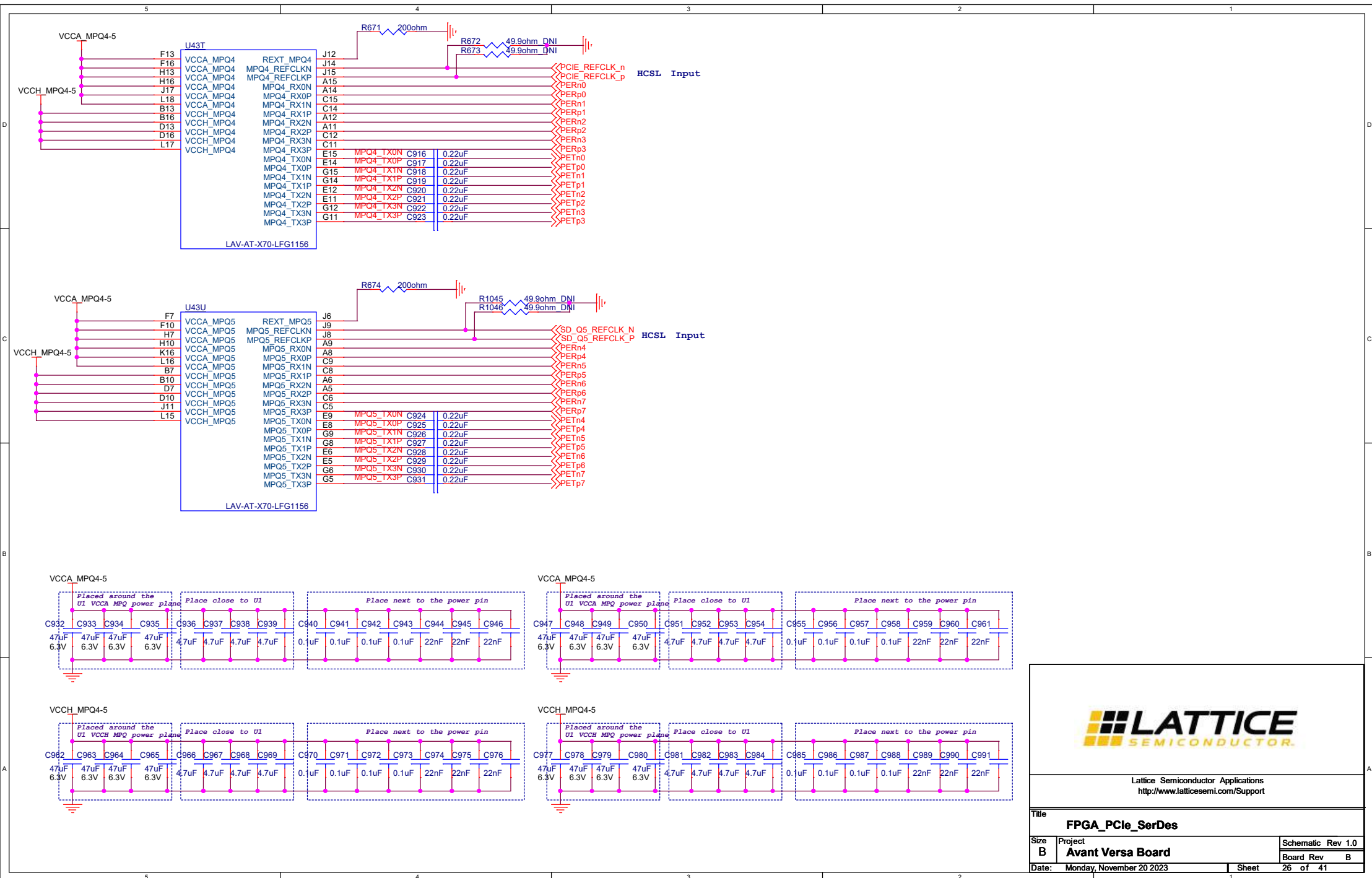
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Size	Project	Avant Versa Board	Schematic Rev 1.0
C	Project	Avant Versa Board	Board Rev B
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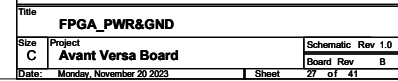
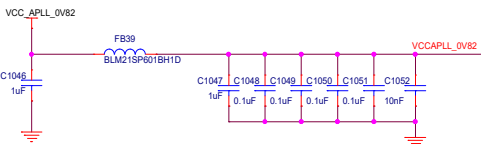
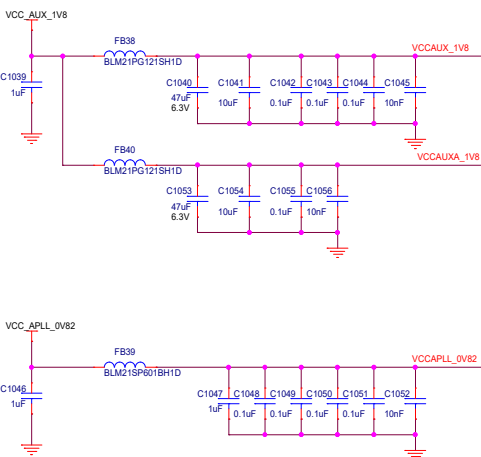
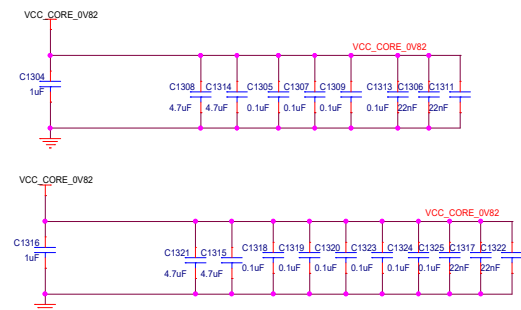
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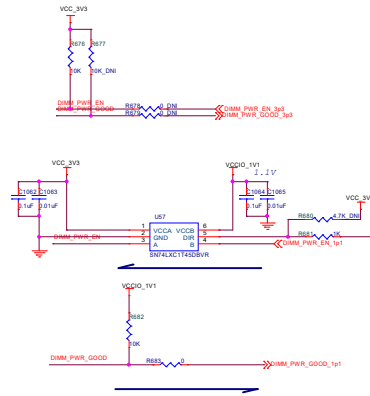
Title			FPGA_25GE&10GE_SerDes
Size	Project	Schematic Rev 1.0	
B	Avant Versa Board	Board Rev	B
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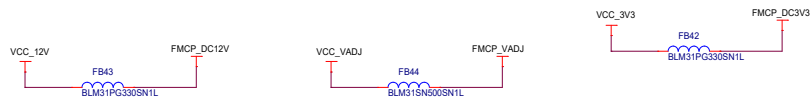
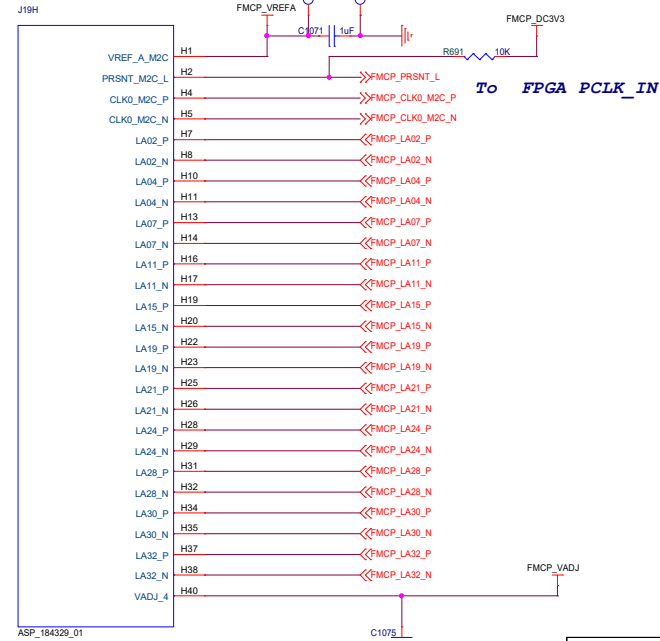
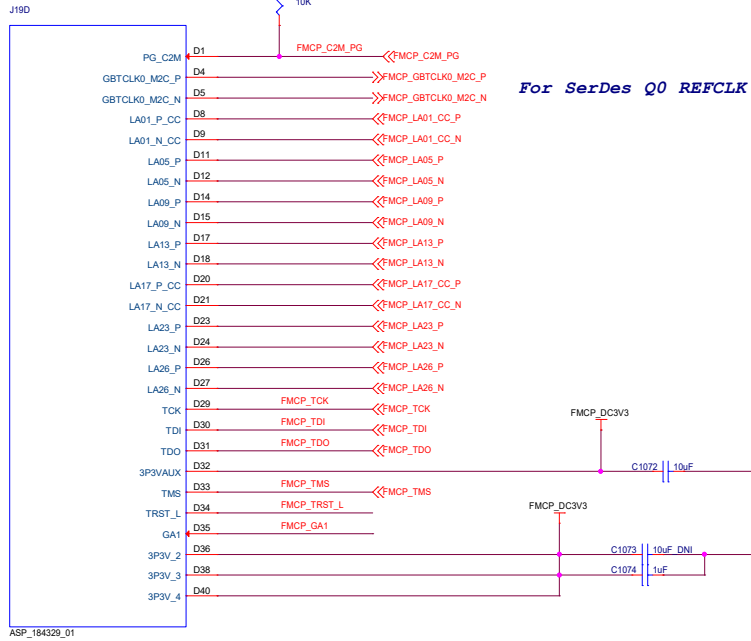
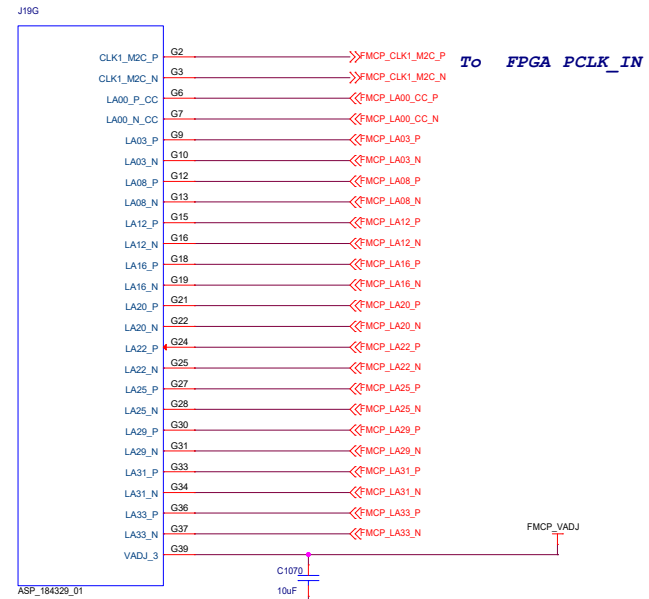
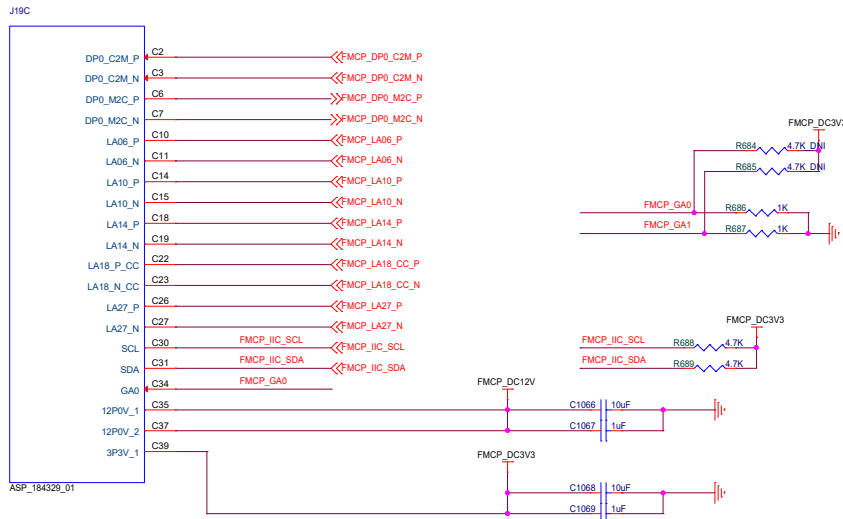


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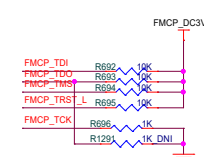
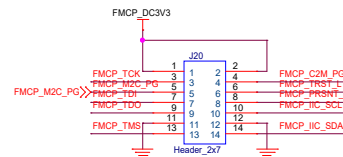
Title			FPGA_PCl_e_SerDes
Size	Project	Schematic Rev 1.0	
B	Avant Versa Board	Board Rev B	
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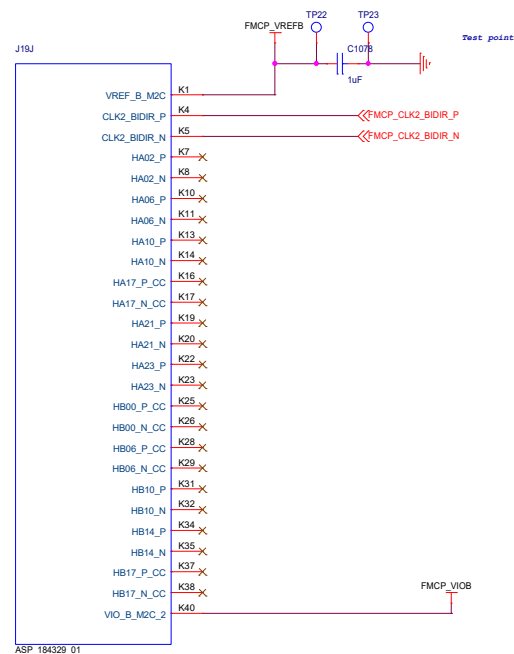
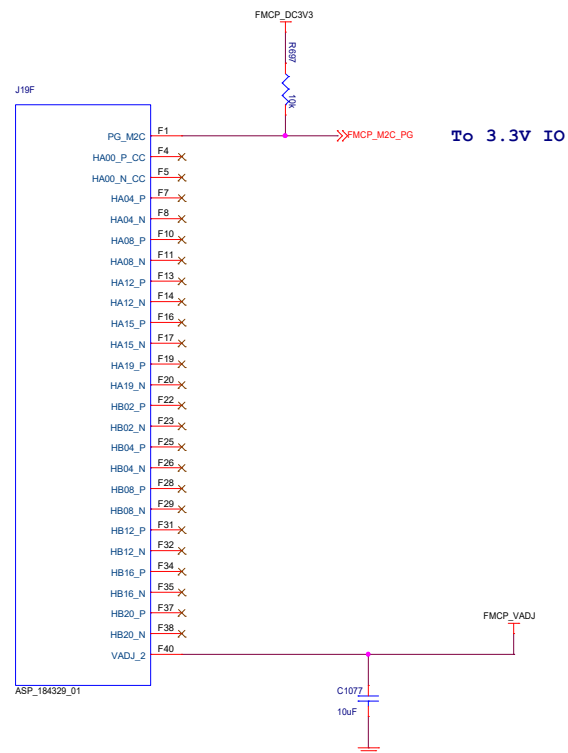
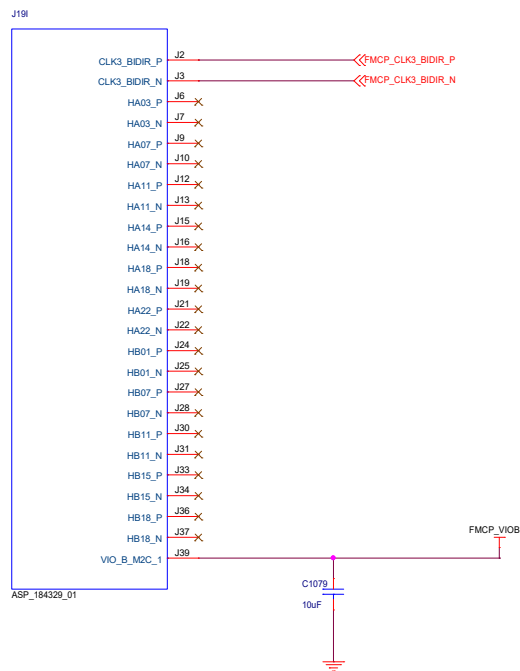
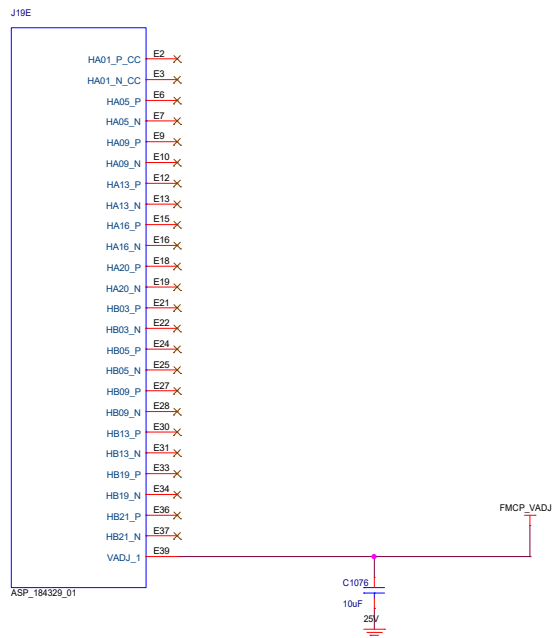


Parallel FMC CFG Header



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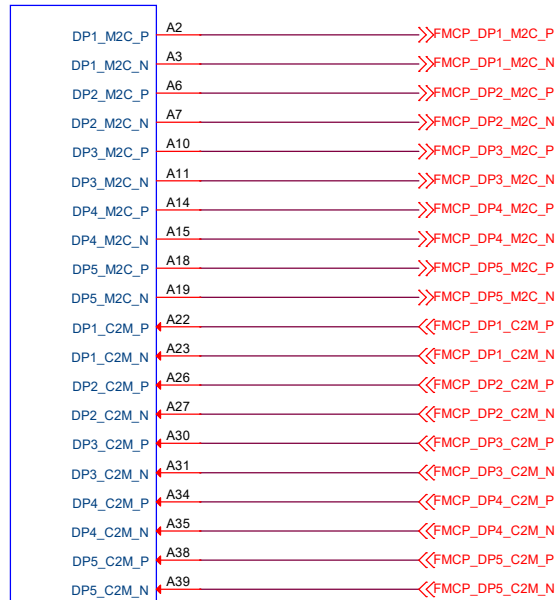
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Size	Project	Avant Versa Board	Schematic Rev 1.0
C	Board Rev	B	
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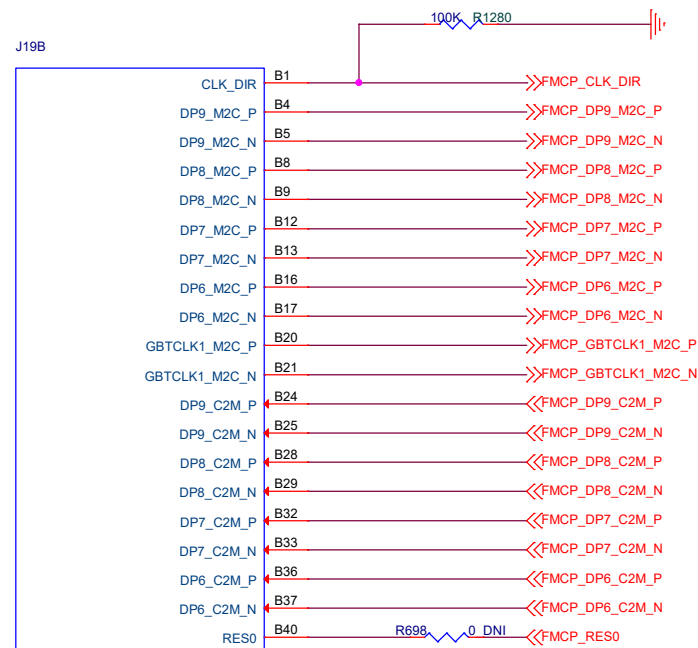
Title			FMCP_HSPC2
Size	Project	Schematic Rev 1.0	
C	Avant Versa Board	Board Rev B	
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J19A



ASP_184329_01

J19B



ASP_184329_01

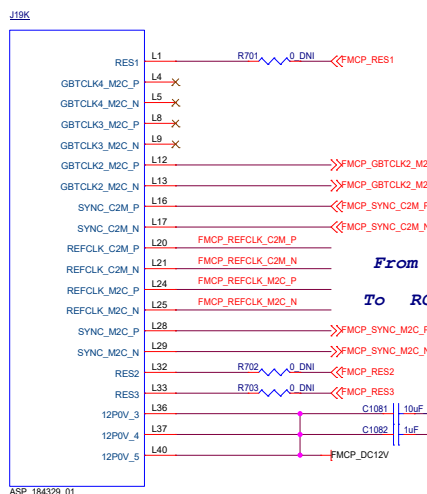
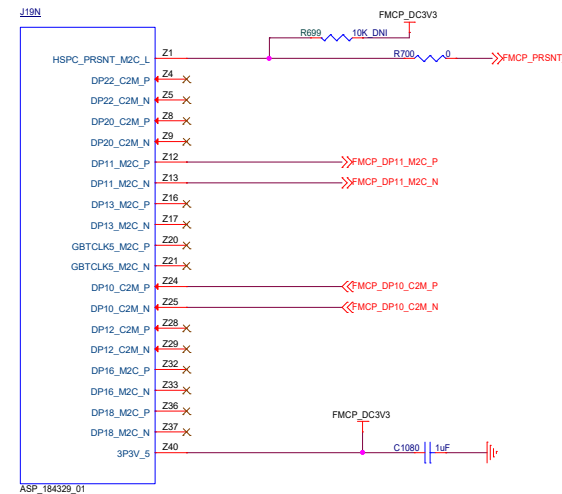
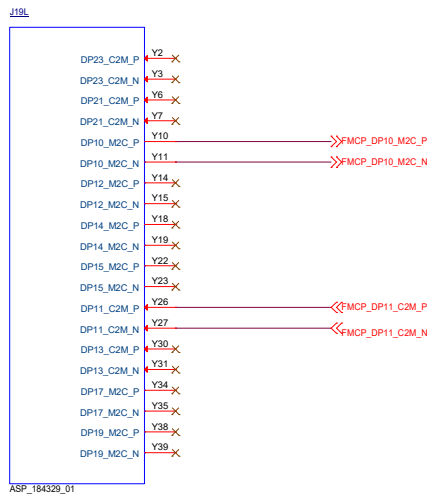
For SerDes Q1 REFCLK

All AC coupling for the DP signals will all be placed on the mezzanine card. No AC coupling will be placed on the carrier card.



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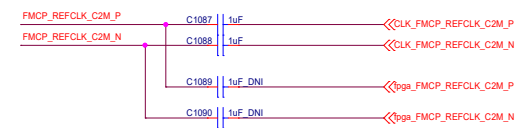
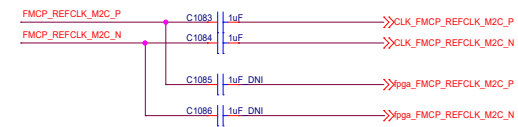
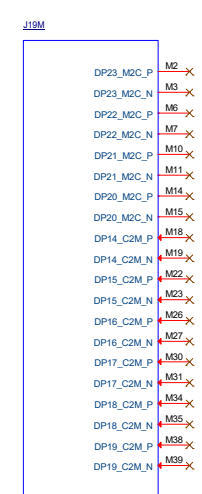
Title FMCP_HSPC3			
Size B	Project Avant Versa Board	Schematic Rev 1.0	
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For SerDes Q2 REFCLK

From RC38612 OUT, Optional from FPGA CLKOUT

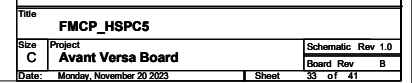
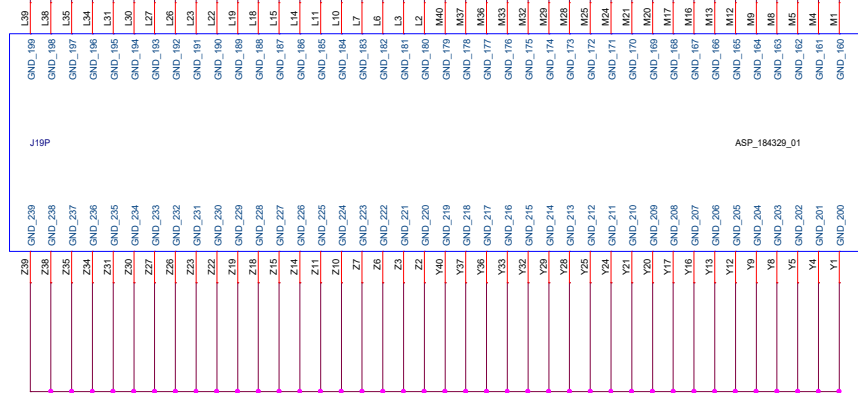
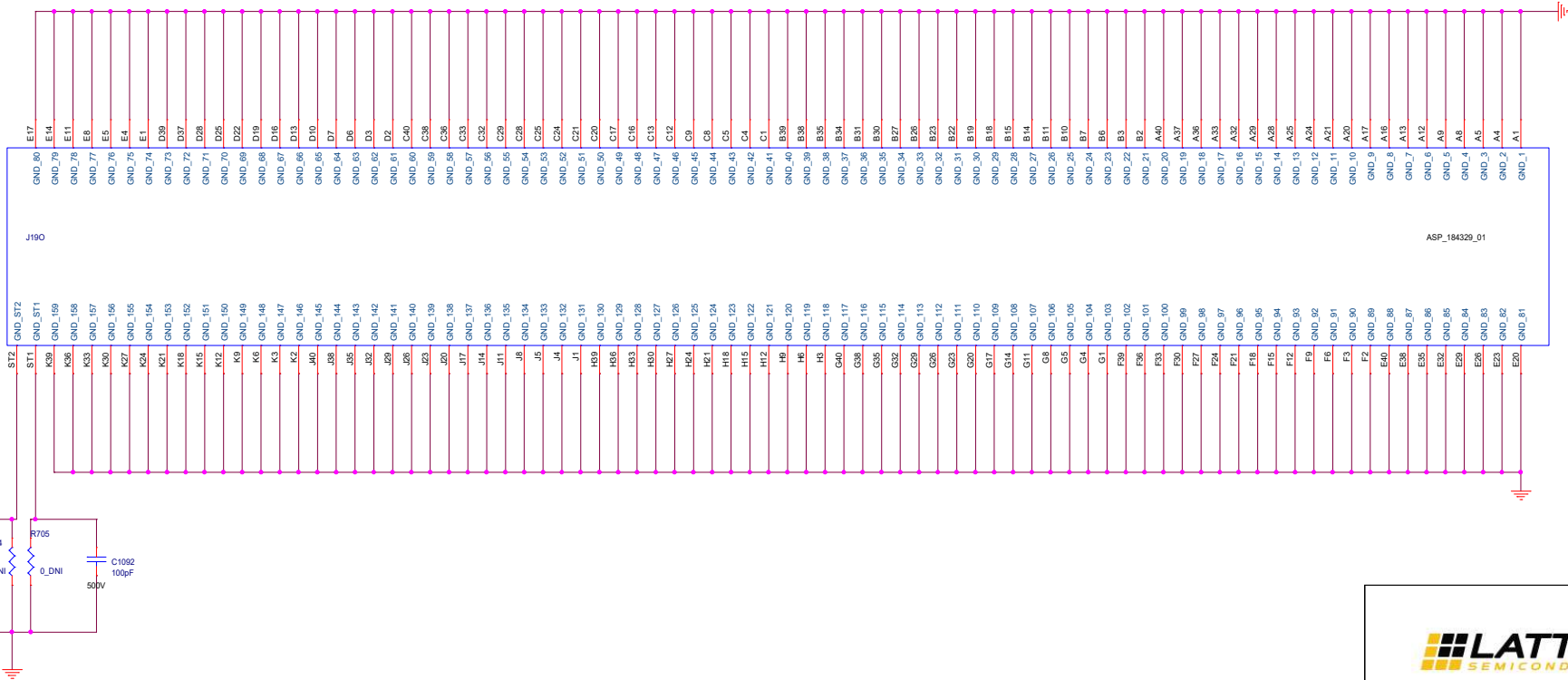
To RC38612 CLK_IN, Optional to FPGA IO





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Title FMCP_HSPC4		
Size C	Project Avant Versa Board	Schematic Rev 1.0
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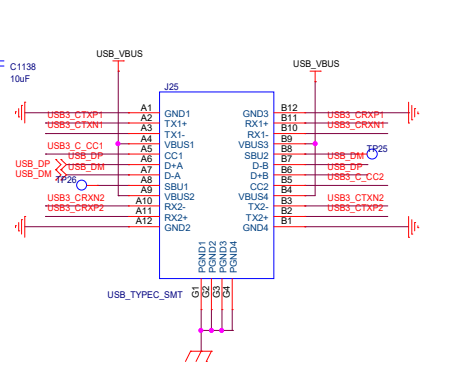
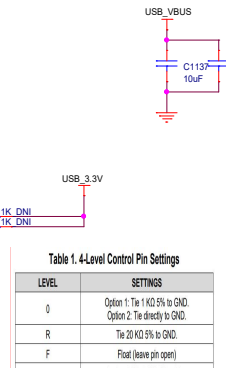
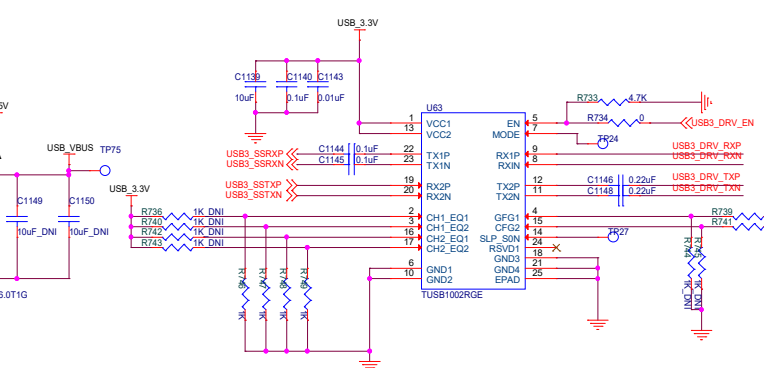
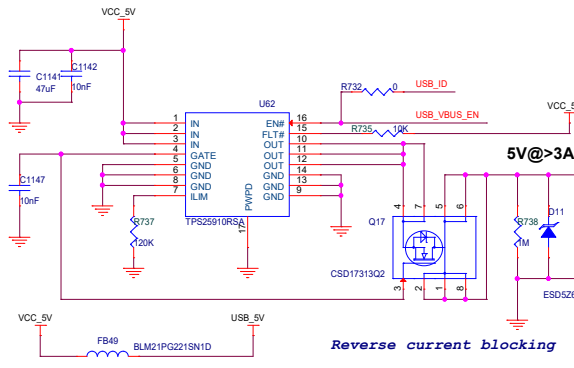
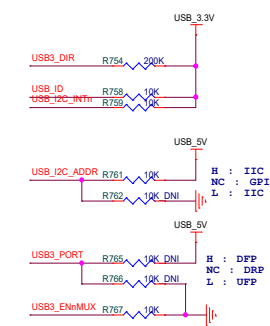
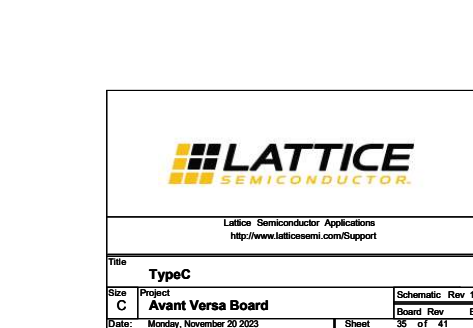
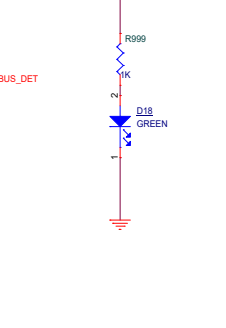
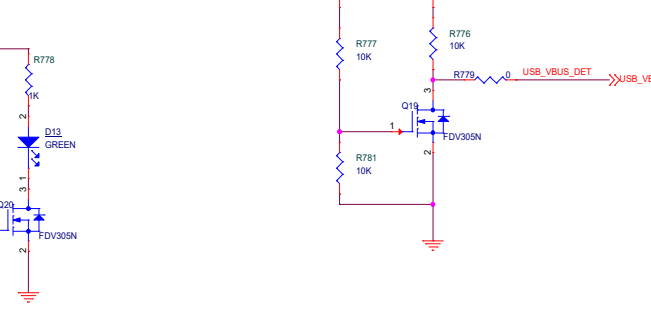
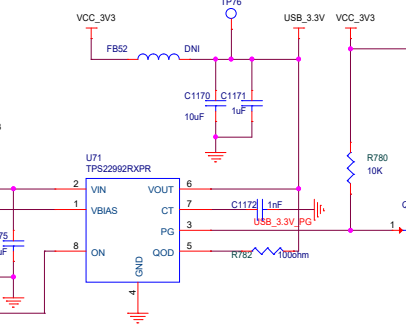
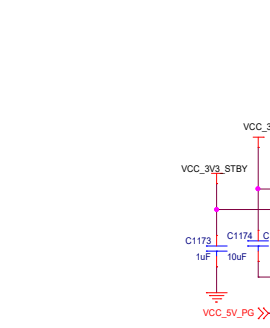
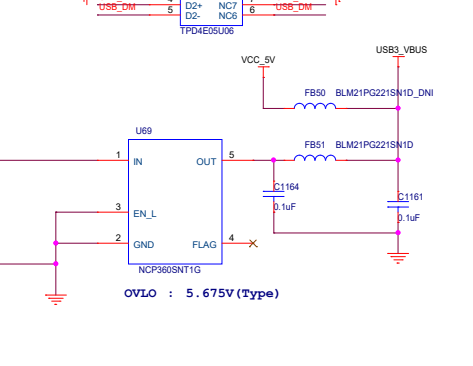
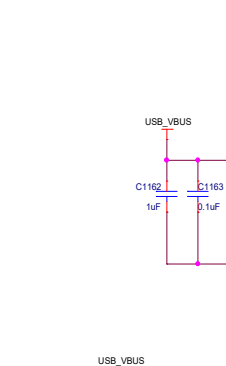
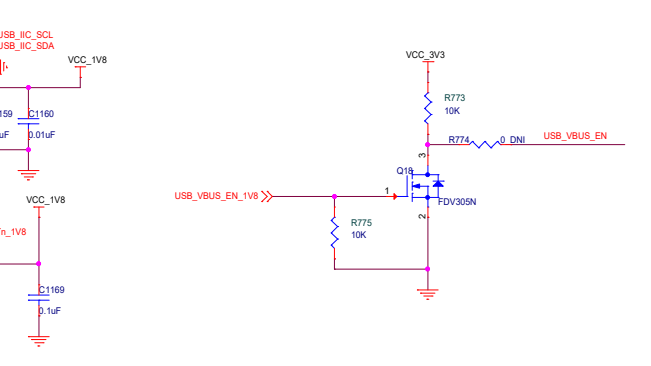
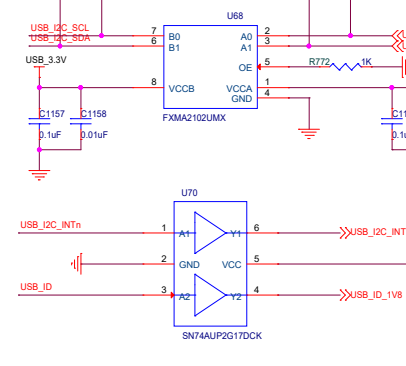
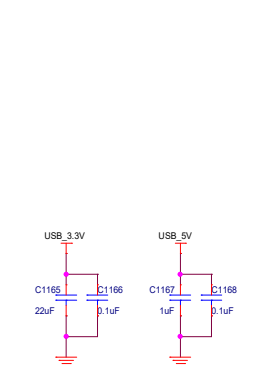
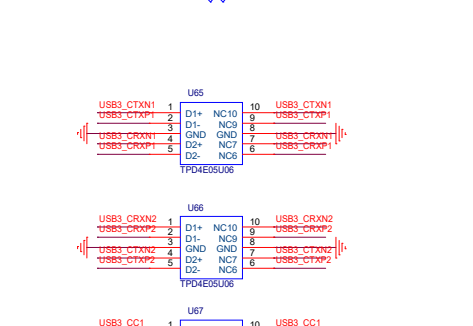
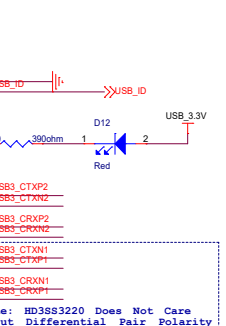
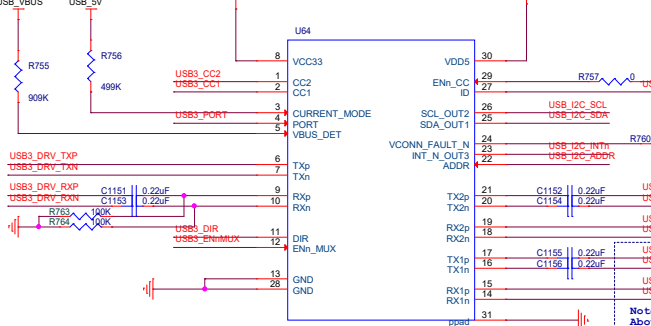


Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open).
1	Option 1: Tie 1 KΩ 5% to V _{CC} . Option 2: Tie directly to V _{CC} .



Current_mode:
L - Low - Default : 900 mA
M - Medium (Install 500 K to VDD on the PCB) : 1.5 A
H - High (Install 10 K to VDD on the PCB) : 3 A



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Title: **TypeC**

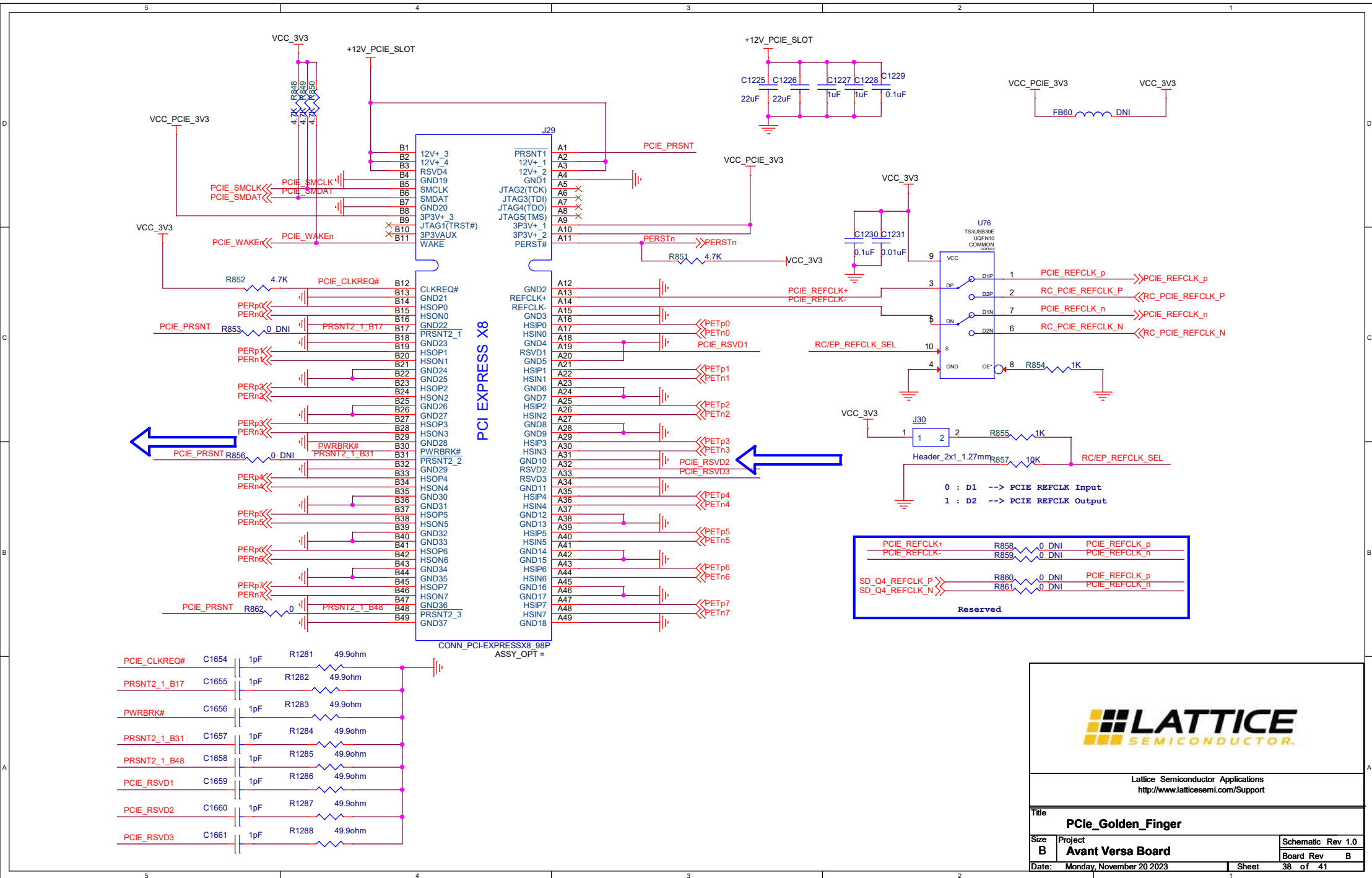
Size: **C**

Project: **Avant Versa Board**

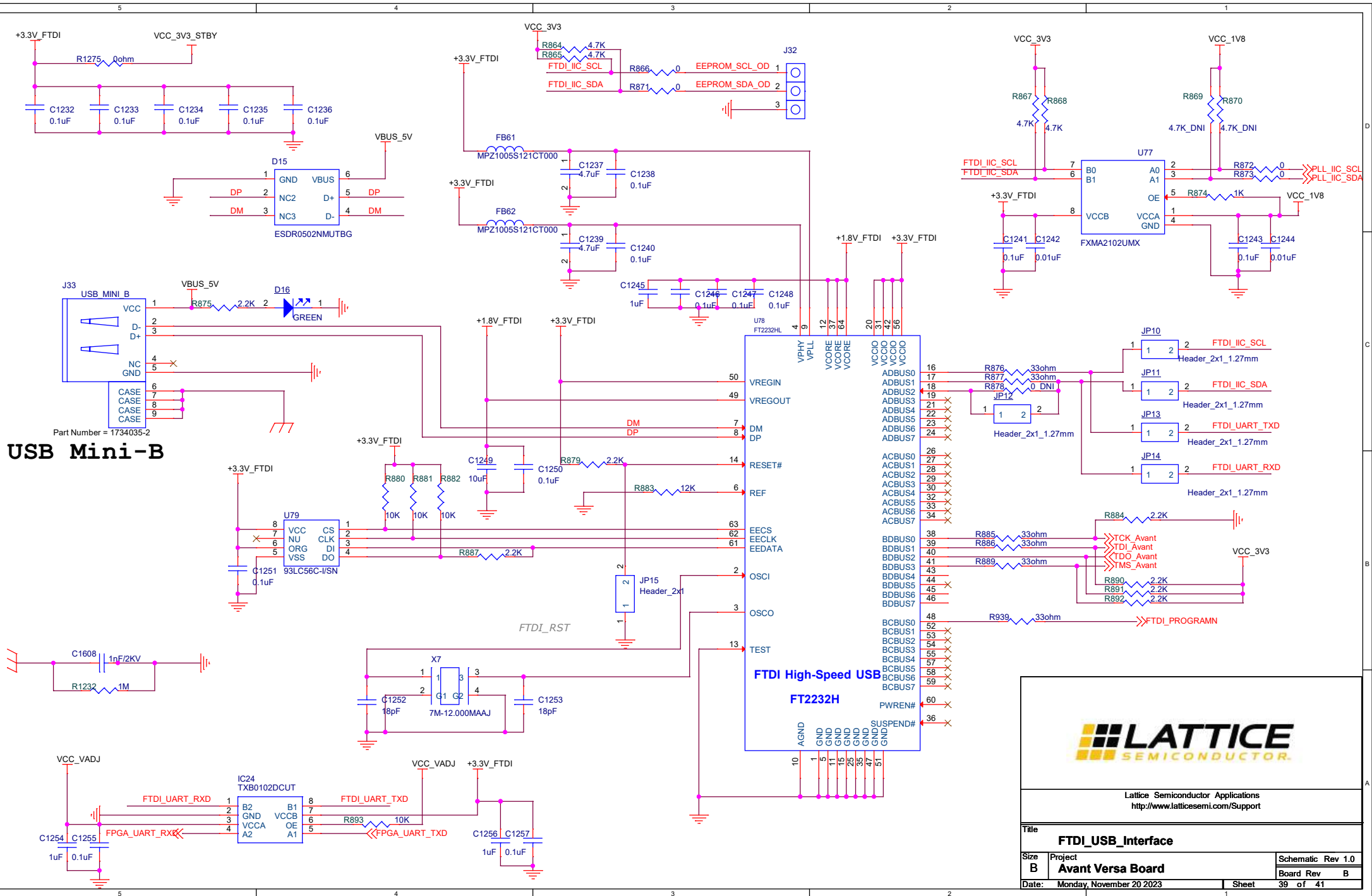
Schematic: **Rev 1.0**

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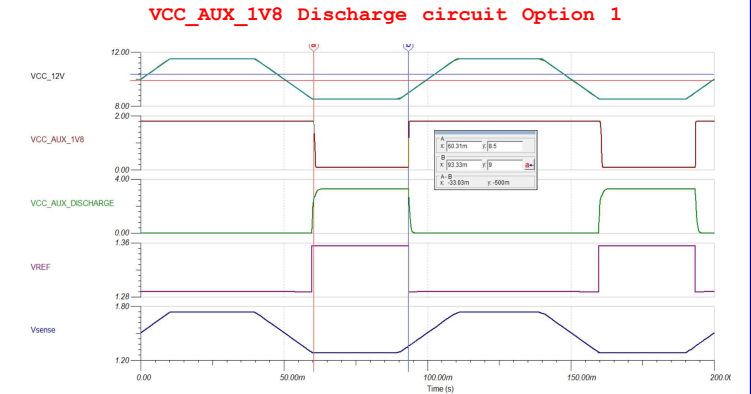
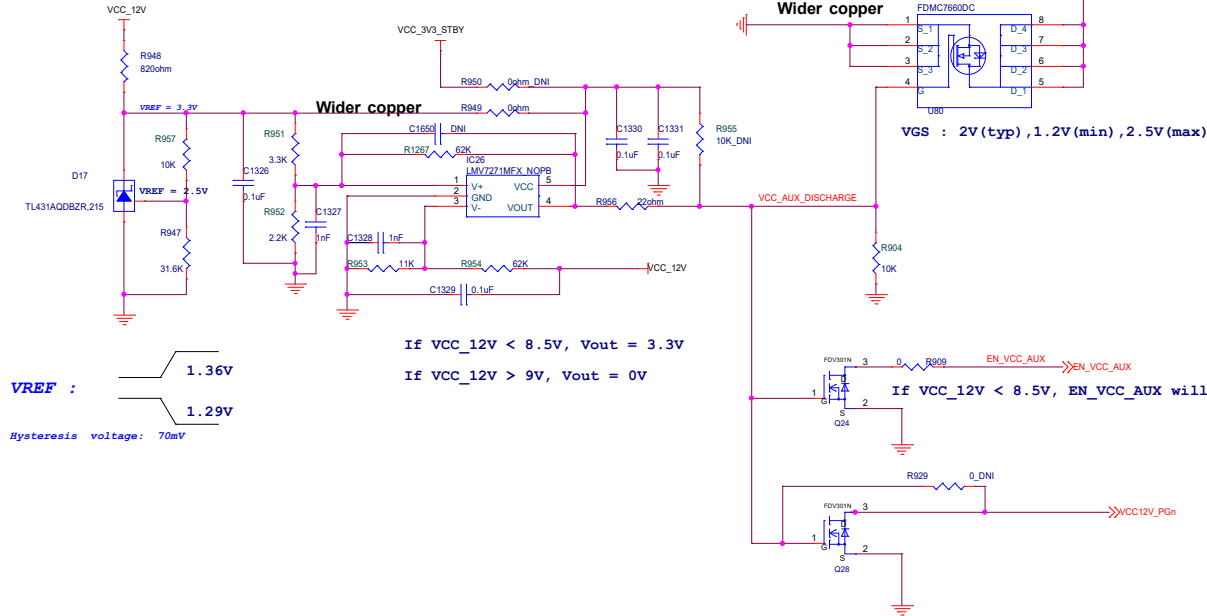


USB Mini-B

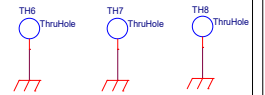
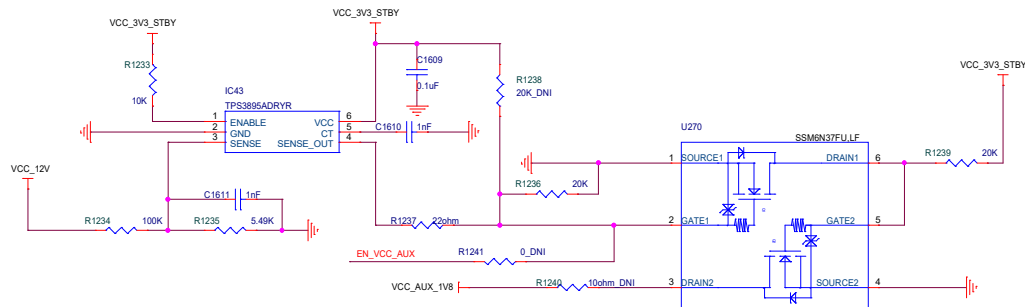


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Size	Project		Schematic Rev 1.0	
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VCC_AUX_1V8 Discharge circuit Option 2



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Revision records from Rev-A to Rev - B :

- 1 : The schematic symbol of U43 has been updated.
VCCCLK and VCCHP have been changed to VCC.
EXT_RES PINs cannot be used as IO.
- 2 : The connection of the R573 has been changed from U43 PIN AA10 to U43 PIN AC9, as PIN AA10 cannot be used as an IO.
Additionally, R1292 has been added to pull up U43 PIN AA10 to VCC 1V8, but it is not installed by default.
- 3 : The test point TP81 has been added to test the voltage of VCC_APLL 0.82V.
The test point TP82 has been added to test the voltage of VCC_AUX 1.8V.
- 4 : The name of the nets was changed from BANK8_REFCLK_P&BANK8_REFCLK_N to BANK7_REFCLK_P&BANK7_REFCLK_N,
but the traces routing on the PCB was not modified.
- 5 : The net zSFP1_LINK_LED was interchanged with the net zSFP2_LINK_LED.
The net zSFP1_LED was also exchanged with the net zSFP2_LED.
However, there were no modifications made to the traces routing on the PCB.
- 6 : A 1Kohm pull-down resistor (R1291) is reserved to be connected to FMC_TDO (U43 PIN W2).
It is not installed by default.
- 7 : The values of R179, R193, R996, R997, and R998 have been changed to 0_DNI.
- 8 : Deleted FB66 , FB67 , FB74 .
VCCCLK_0V82 & VCCHP_0V82 have been changed to VCC_CORE_0V82.
- 9 : The schematic symbol of IC2 has been updated. The new symbol is compatible with UCD90120A and UCD90160.



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Title			
History			
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B	Avant Versa Board	Board Rev	B
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