



Nexus MIPI D-PHY Module

IP Version: v1.9.1

Release Notes

FPGA-RN-02105-1.1

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1. Introduction

This document contains the Release Notes for the MIPI D-PHY Module. For specific details about the IP and driver, refer to the following:

- [Nexus MIPI D-PHY Module User Guide \(FPGA-IPUG-02061\)](#)

MIPI D-PHY Module v1.9.1

Software	Software Version	Summary of Changes
Lattice Radiant	2026.1	Removed explicit string parameter size declarations to improve compatibility with software tools starting from the Lattice Radiant software version 2025.2.

MIPI D-PHY Module v1.9.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.2	• Updated maximum data rate of Soft MIPI D-PHY for LFMX05-35, LFMX05-35T, LFMX05-65, LFMX05-65T, LFD2NX-35, and LFD2NX-65 devices. • Improved internal ECLK and SCLK synchronization in Nexus devices for enhanced robustness. • Fixed issues with testbench. • Enhanced constraint generation and implementation using the new IP constraint propagation method by the software. • Other minor IP enhancements and general bug fixes.

MIPI D-PHY Module Earlier Versions

IP Version	Summary of Changes
1.8.0	Updated PLL Module.
1.7.0	Updated internal reset connection of RX Soft MIPI D-PHY.
1.6.0	• Updated internal PLL parameter optimization algorithm. • Added txclk_hsgate_i port. • Updated maximum data rate of Soft MIPI D-PHY for LIFCL-17 and LIFCL-40 devices.
1.5.0	• Added support for UT24C and UT24CP devices. • Updated analog parameter calculation script of Soft MIPI D-PHY internal PLL.
1.4.0	• Added support for LFMX05 devices. • Updated testbench for RX Hard MIPI D-PHY CIL Bypassed mode timing parameters. • Updated calculation script of Soft MIPI D-PHY internal PLL. • Updated constraint file.
1.3.0	• Updated metadata and plugin to support new IP Engine. • Updated PLL rtl. • Removed <i>lsc_dphy_rx_model.v</i> file on testbench folder. • Updated <i>tb_top.v</i> interface clock period. • Updated initial value of Hard D-PHY test pattern attribute. • Added hs_rx_clk_en_i and hs_rx_data_en_i as separate termination enable ports for clock and data. • Added data deserializer port, hs_data_des_en_i.
1.2.0	• Updated PLL. Added parameter setting for DIV_DEL. • Updated Soft MIPI D-PHY internal PLL analog parameter calculation.
1.1.1	Added support for LFCPNX devices.
1.1.0	Updated PLL instance.
1.0.2	Added support for LFD2NX devices.

IP Version	Summary of Changes
1.0.1	Updated for SP1.
1.0.0	Initial release.

References

- [Nexus MIPI D-PHY Module User Guide \(FPGA-IPUG-02061\)](#)
- [CrossLink-NX](#) web page
- [Certus-NX](#) web page
- [CertusPro-NX](#) web page
- [MachXO5-NX](#) web page
- [Lattice Radiant Software](#) web page
- [Lattice Propel Design Environment](#) web page
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

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For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.



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