

LFCPNX-SOM-EVN

Rev - C

01 - Title Page

02 - Block Diagram

03- CPNX_Bank_0 &3

04- CPNX_Bank_1 &2

05- CPNX_Bank_4,5,6

06- CPNX_SERDES

07- Connector

08- XO3D FPGA

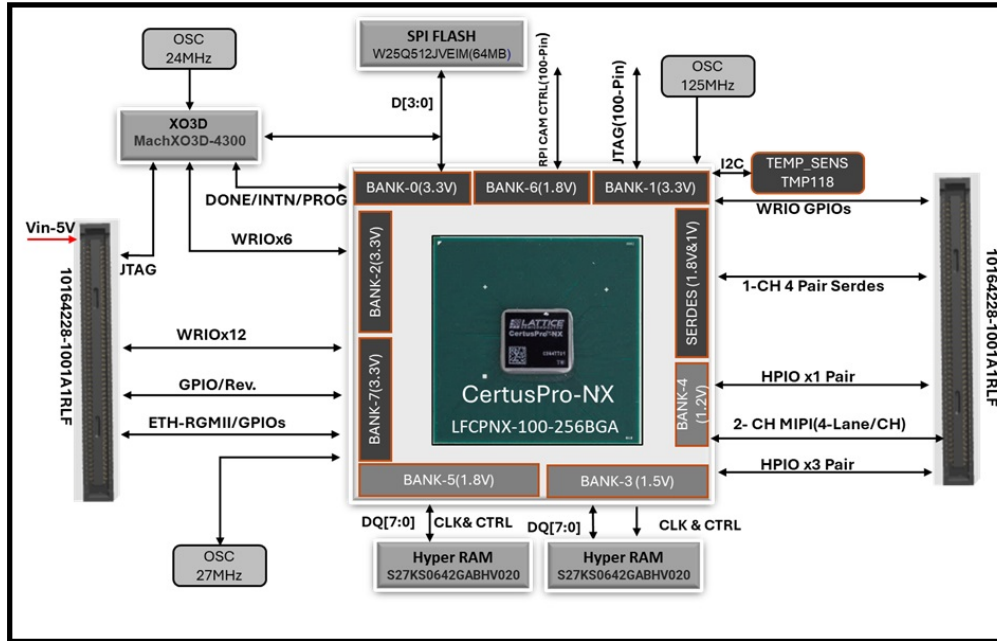
09- Power Supply

10- Power Diagram

<Variant Name>



BLOCK DIAGRAM



<Variant Name>



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Title
Block Diagram

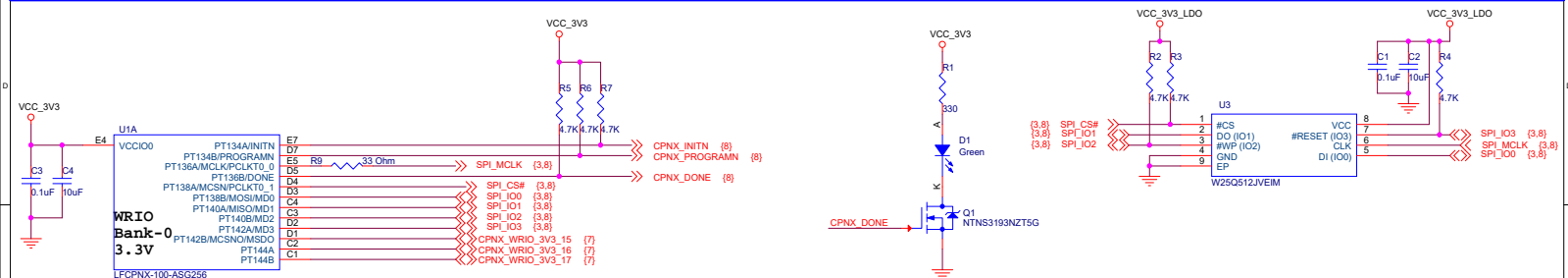
Size B Project LFCPNX-SOM-EVN

Date: MAR 26, 2021

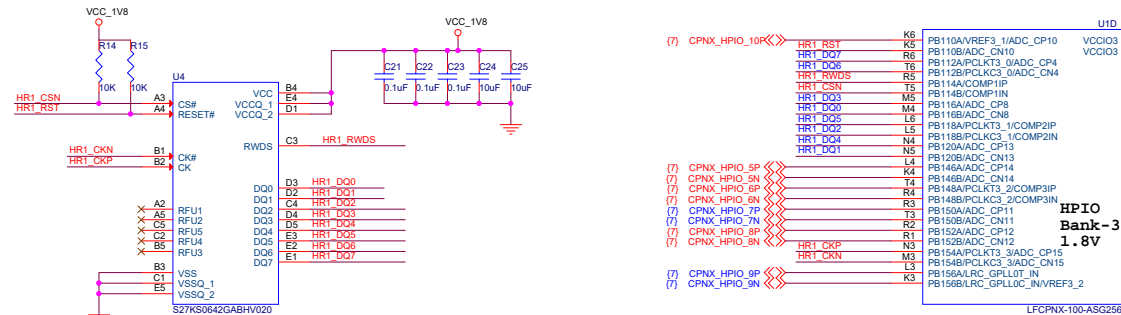
Schematic Rev 2.0
Board Rev C

Sheet 2 of 10

FPGA CONFIGURATION



HYPERRAM INTERFACE



<Variant Name>



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Title	CPNX Bank 0 Config
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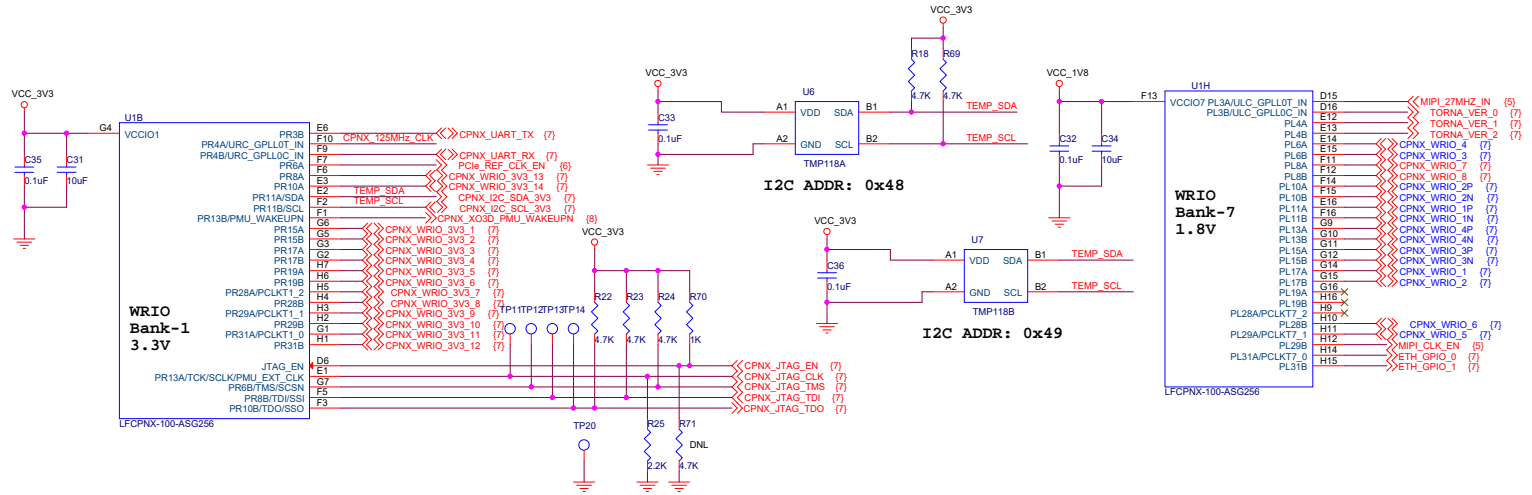
Size B	Project LFCPNX-SOM-EVN
-----------	----------------------------------

Schematic Rev	2.0
Revised By	2

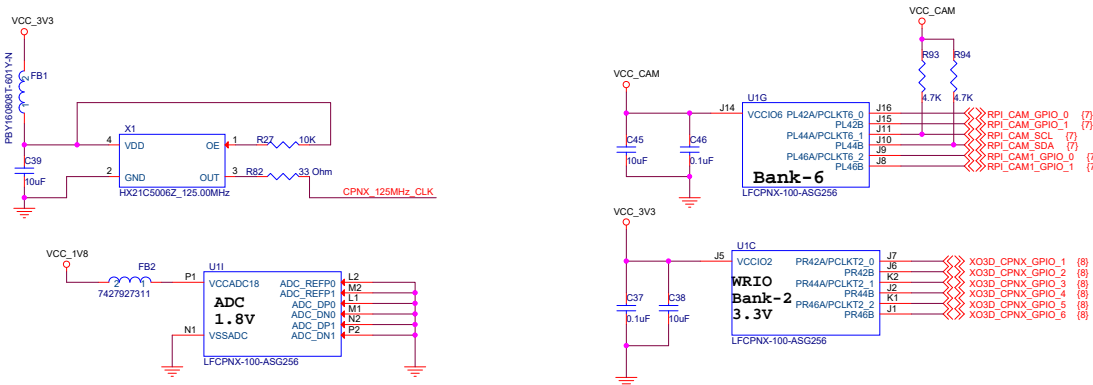
Date: MAR 26, 2021

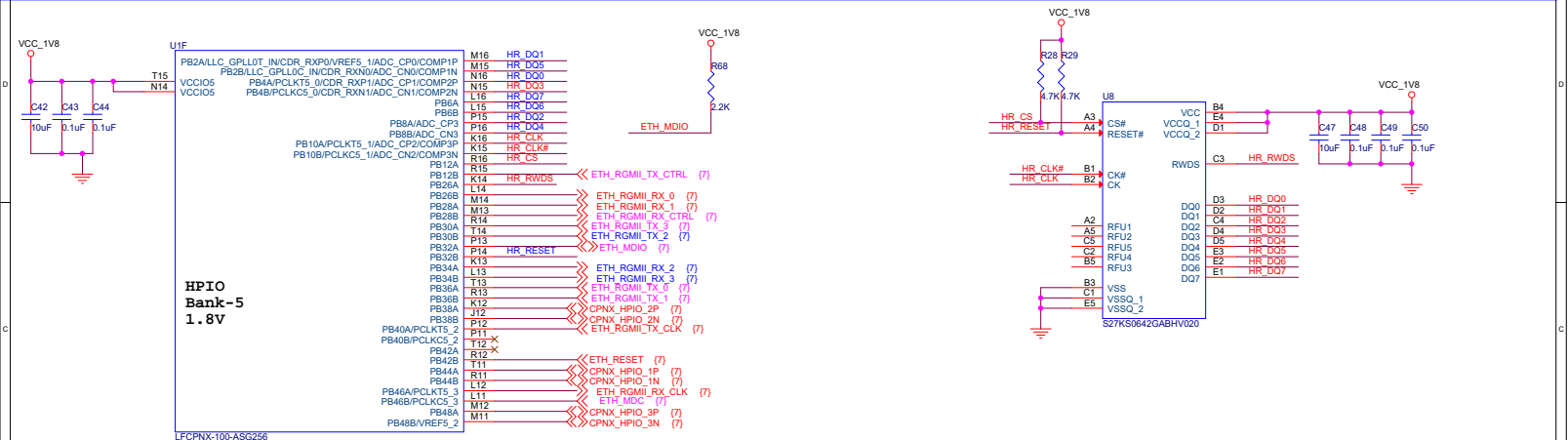
Sheet	3	of	10
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JTAG , TEMP SENS & WRIO INTERFACE

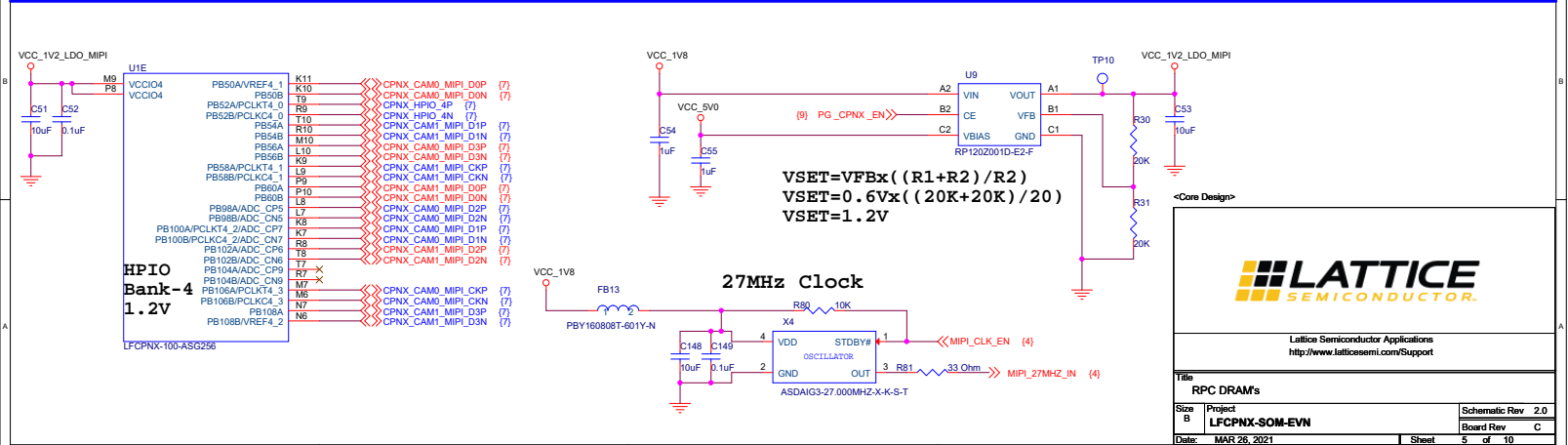


CLOCK & ADC INTERFACE

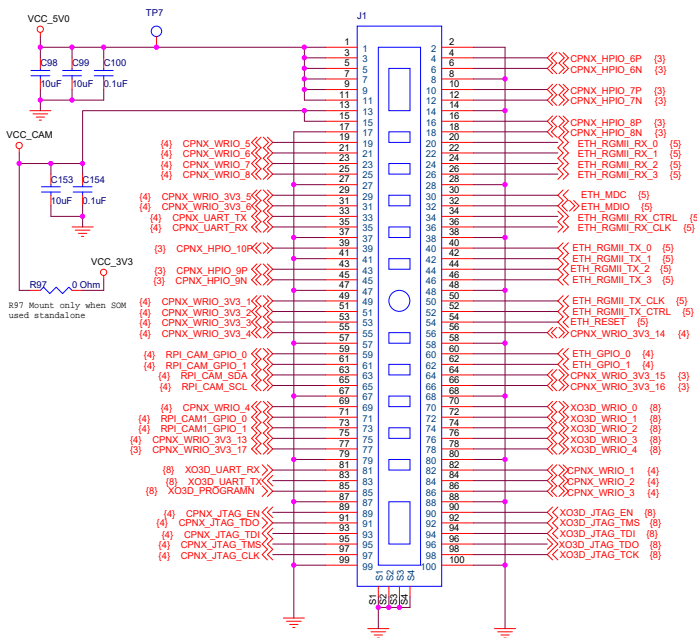




MIPI CAMERA INTERFACE

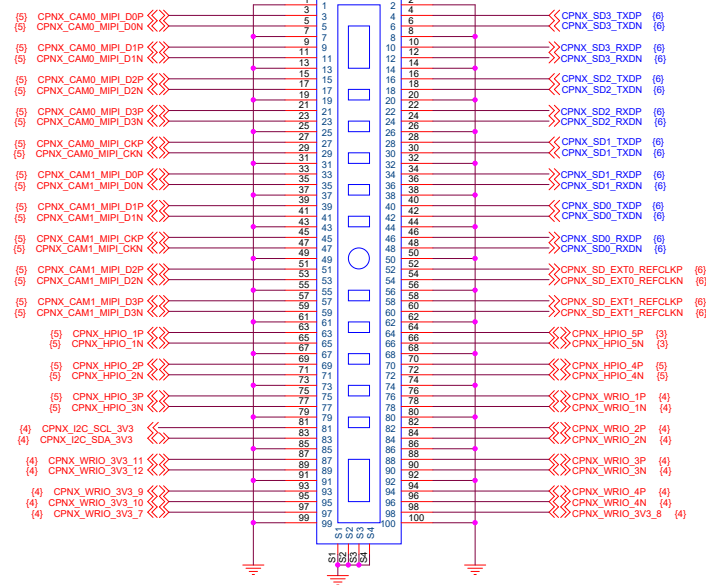
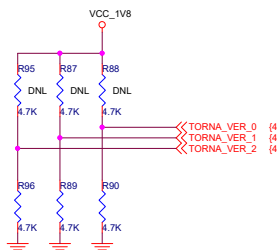


100-PIN CONNECTOR



10164228-1001A1RLF

Board Version Control



10164228-1001A1RLF

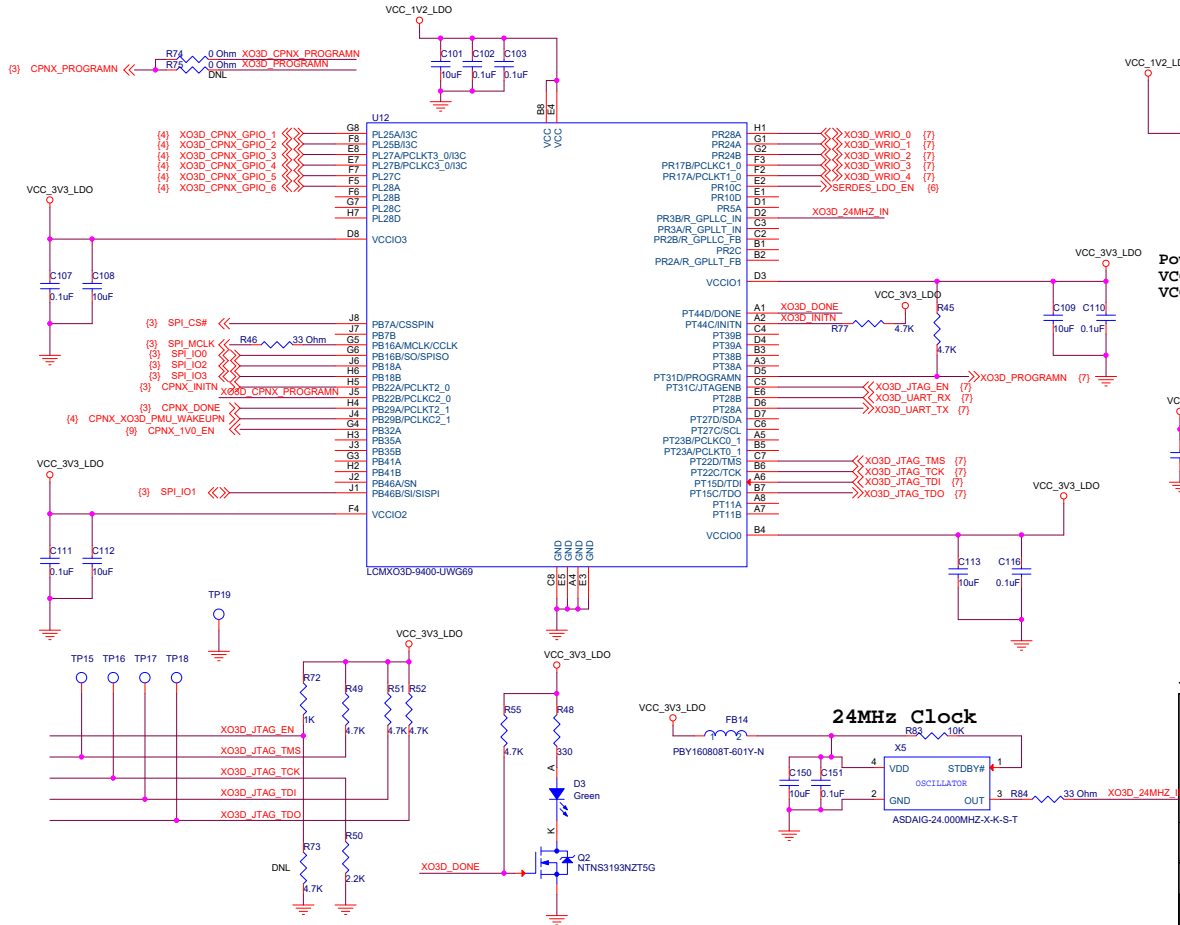
<Variant Name>



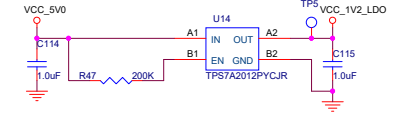
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Title		B2B Connector	
Size	Project	LFCPNX-SOM-EVN	
Date:	MAR 28, 2021	Sheet	7 of 10

X03D FPGA



Power Sequence X03D: For HE devices, VCC needs to be powered up prior to VCCIOx by at least 20 ms.



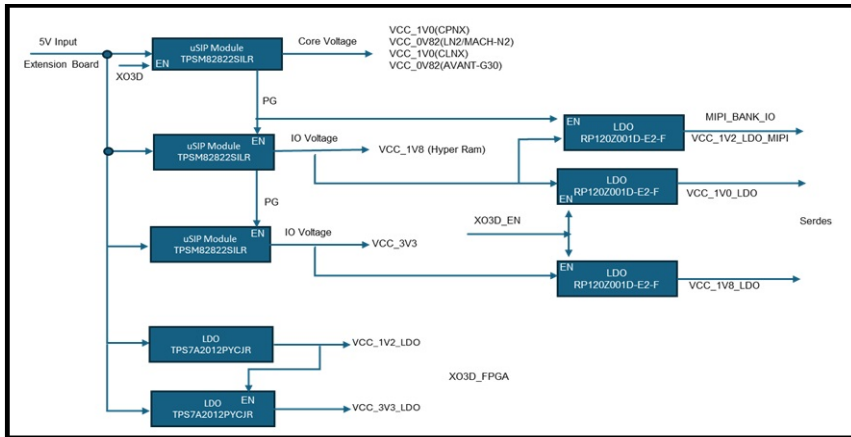
<Core Design>



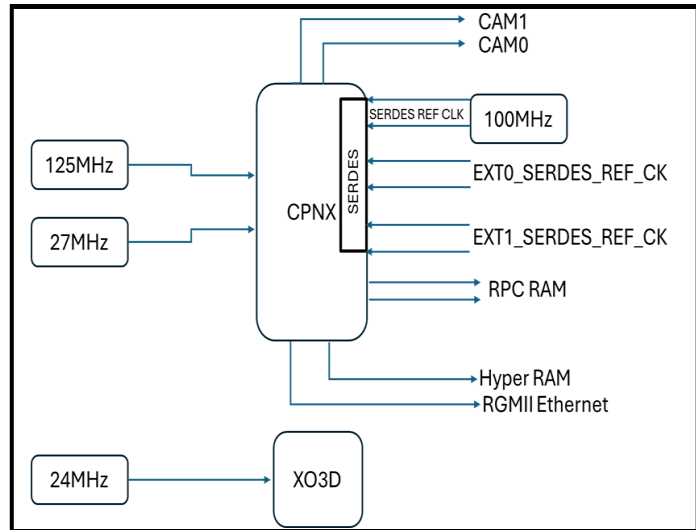
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Title			
X03D FPGA			
Size B	Project LFCPNX-SOM-EVN	Schematic Rev 2.0	
		Board Rev C	
Date:	MAR 26, 2021	Sheet	8 of 10

POWER TREE



CLOCK Diagram



<Core Design>



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Title		
Power Diagram		
Size B	Project	Schematic Rev 2.0
	LFCPNX-SOM-EVN	Board Rev C
Date: MAR 28, 2021	Sheet	10 of 10