Lattice Radiant 2023.2.1 Software Release Notes

Welcome to Lattice Radiant™ software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2023.2.1 Software

- **Device Support:**
  - CertusPro™-NX (LFCPNX)
    - 50K (-9/-8/-7) 1.0V (AUTO) – ASG256, CBG256, BFG484.
  - Certus™-NX (LFD2NX)
    - 40K (-9/-8/-7) 1.0V (COM/IND) – CABGA196.
  - MachXO5™-NX (LFMXO5)
    - 15D (-8/-9) 1.00V (COM/IND) – BBG256.
    - 15D (-8/-9) 1.00V (COM/IND) – BBG400.
    - A special license is required to access features of the LFMXO5-15D device. To request for a license, you may raise a ticket to the Submit Support Ticket page.

Tool and Other Enhancements:

- **Primitives**
  - OUTDELAYC primitive has been added for CertusPro-NX device.

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- **Device Constraint Editor**
  - 75Mhz selection has been added for MCCLK_FREQ.
- **MAP** – DRC errors regarding shared configuration pin usage for Nexus devices have been resolved.
- **Timing Data** – DPHY timing arcs to fix unconstrained path have been updated for Nexus device.

- **Reveal**
  - JTAGhub feature modules have been enhanced for Nexus and Avant devices.
  - Pooling of data while SEDC is running has been enhanced for Reveal Controller and Reveal Analyzer.
- **Hardware Data File**
  - Minimum pulse width (MPW) has been aligned with datasheet for CrossLink-NX device.
  - Correlation for CertusPro-NX (LFCPNX) IBIS Model has been resolved.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP			IP Regeneration Procedures
	Avant (LAV-AT-E)	**CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**iCE40UP**	
2023.2.1	RAM_DQ	MPCS	N/A	These IP used in designs created in Radiant 2023.2 or earlier must be re-generated in Radiant 2023.2.1
	RAM_DP	RAM_DQ		
	RAM_DP_True	RAM_DP		
	ROM	RAM_DP_True		
	FIFO	ROM		
	FIFO_DC	FIFO		
		FIFO_DC		

The following server IP are not compatible with Radiant 3.0 onwards. Use the latest versions of the IP available on the IP server:

- I2C Master version 1.0.3
- UART 16550 version 1.0.4
- DDR3 SDRAM Controller version 1.1.1
- DDR3 SDRAM Controller version 1.2.1
- LPDDR2 SDRAM Controller Lite version 1.1.1
- LPDDR2 SDRAM Controller Lite version 1.2.1

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus™ (iCE40UP)	◄	
Lattice Avant™ (LAV-AT)		◄
CertusPro-NX (LFCPNX)	Evaluation Mode	◄
Certus-NX (LFD2NX)	◄	
MachXO5-NX (LFMXO5)	Evaluation Mode	◄
CrossLink-NX (LIFCL)	◄	
Certus-NX-RT (UT24C)		RT Subscription
CertusPro-NX-RT (UT24CP)		RT Subscription

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and Siemens ModelSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version U-2023.03LR-SP1**
  - Release Notes for Synplify Pro is located in

    ..\<*install_directory*>\radiant\2023.2\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro is also located in ..\<*install_directory*>\radiant\2023.2\synpbase\doc\.
- **Siemens ModelSim Lattice Edition 2023.3 revision 2023.07**
  - Release Notes for ModelSim Lattice Edition are located in ...\<*install_directory*>\radiant\2023.2.\modeltech\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.

- A full set of documents for ModelSim Lattice Edition is located in ...\<*install_directory*>\radiant\2023.2\modeltech\doc\.

- **Siemens Questa® 2022.3**
- **Cadence Xcelium®**
  - The devices listed below are compatible with the following versions of Xcelium:
    - **23.03.003** – LAV-AT
    - **20.09.012 or earlier versions** – LFCPNX, LFD2NX, LFMXO5, LIFCL, UT24C, and UT24CP
- **Synopsys VCS® U-2023.03-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the 

"Getting Started" icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	ModelSim
Windows 10	✓	✓	✓
Windows 11	✓	✓*	✓*
Red Hat Enterprise Linux 7.9	✓	✓	✓
Red Hat Enterprise Linux 8.8	✓	✓	✓
Ubuntu version 18.04 LTS	✓	✓*	✓*
Ubuntu version 20.04 LTS	✓	✓*	✓*

64-bit OS	Radiant	Synplify Pro	ModelSim
CentOS 7.9	✓	✓	✓*
CentOS 8.4	✓	✓	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50 GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - Avant – 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity.
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed

The following known issues are fixed in this release. Their workarounds are no longer needed.

Resource usage may increase when you migrate your design from Radiant 2023.1 to 2023.2.

Devices affected: MachXO5-NX (LFMXO5-15D)

Bug number: DNG-20179

Fixed in Radiant 2023.2.1

Bitstream generation fails when selecting either "Hex File" or "NVCM File" formats in the Bitstream Settings menu.

Devices affected: iCE40 UltraPlus (iCE40UP)

Bug number: DNG-19371

Fixed in Radiant 2023.2.1

“Child Process Exited Abnormally” error occurs when compiling libraries using Xcelium version 23.03.003.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-18594, DNG-19007

Fixed in Radiant 2023.2.1

IBIS generated string for MCLKP/N always sets the PULLMODE value to None.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19472

Fixed in Radiant 2023.2.1

A rev_* folder is generated each time Synthesis is run in a VHDL design.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-19150

Fixed in Radiant 2023.2.1

Common Path skew computation for clock domain crossing paths caused hold timing violation.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-20114

Fixed in Radiant 2023.2.1

Clock drift in long simulation run results in packet corruption.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-19114

Fixed in Radiant 2023.2.1

DDR placement issue of Place and Route not accepting pin constraints used in a previously successful run.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20456

Fixed in Radiant 2023.2.1

Fixed DRC check for data rate attribute error for MPCS IP.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-20415

Fixed in Radiant 2023.2.1

VHDL 2008 option under Project > Active Strategy > Synplify Pro settings not working after it is set to “TRUE”.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19928

Fixed in Radiant 2023.2.1

VCS issuing “[IND] Identifier not declared” error on cae_library/simulation/verilog/lifcl/lmmis_init_fsm.v when running simulation on LIFCL design in Linux.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-19861

Fixed in Radiant 2023.2.1

FIFO Memory Modules IP for Avant device is not working in FWFT mode.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-20406

Fixed in Radiant 2023.2.1

Long readback time from SRAM through JTAG when using Programmer for Avant family devices.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19817

Fixed in Radiant 2023.2.1

When using SEDC module from the IP Catalog, or when instantiating the SEDCA primitive, the "sedc_busy_o" (IP) or "SEDCBUSY" (primitive) signal will not assert in simulation.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19456

Fixed in Radiant 2023.2.1

Memory initialization for Propel design through ECO Editor is not functional.

Devices affected: All devices

Bug number: DNG-18316, DNG-18383, DNG-18001

Fixed in Radiant 2023.2.1

Synplify Pro crash on specific hardware configurations with Ubuntu 20.04 due to Synplify library issue.

Device affected: All devices

Bug Number: DNG-15909

Fixed in Radiant 2023.2.1

Synplify Pro program error occurs when synthesizing standard_logic_vectors adders of specific width.

Devices affected: Lattice Avant (LAV-AT)

Bug Number: DNG-19556

Fixed in 2023.2.1

Program error occurs for Lattice Radiant while opening the Power Calculator.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20708

Fixed in 2023.2.1

Synplify Pro Lattice OEM (*.srr and *.srf files) may incorrectly report the number of LRAMs for the target device.

Devices affected: CertusPro-NX (LFCPNX-50)

Bug number: DNG-16362

Fixed in 2023.2.1

The SED block reports an error when a distributed RAM is partially used in the design.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-18424

Fixed in 2023.2.1

Errata: Known Issues Identified After Radiant 2023.2.1

Applicable to: R2023.2 SP1 Release

This Errata lists issues identified after the official R2023.2 SP1 release. It is maintained as a living document and updated whenever a new issue impacting R2023.2 SP1 is identified.

Important Note:

- Please review this section before your safety release.
- Each Known Issue includes a "Fixed Version" field:
  - Fixed – specifies the exact version where it was resolved (e.g., "Fixed in R2024.1")
  - Not fixed – set to "future Radiant release"
- The workarounds documented in this section are not tested for use in the functional safety application. Therefore, it is the user's responsibility to test them in the safety application.

Radiant Programmer/Deployment Tool generates an incorrect STAPL during the “Erase, Program, Verify, Refresh” provisioning sequence, causing a false error.

Devices Affected: MachXO5 (LFMXO5)

Bug Number: DNG-24335

Fixed Version: R2024.2

Large Difference in LUT4 Resource Usage Between Synplify Pro and LSE

When synthesizing the same design, users may observe a significant difference in LUT4 MAP resource utilization between Synplify Pro and Lattice Synthesis Engine (LSE).

Analysis shows that this discrepancy originates in the post-synthesis netlist, prior to mapping, and is caused by the different optimization and logic-mapping algorithms used by the two synthesis tools. As a result, MAP may report noticeably different LUT4 usage depending on the chosen synthesizer.

Devices Affected: CertusPro-NX (LFCPNX)

Bug Number: DNG-23772

Fixed Version: R2024.2

Radiant may incorrectly use create_clock instead of create_generated_clock for the PCIe x4 IP clk_usr_o, leading to incorrect timing analysis and unstable PAR results across compilations

Incorrect autogenerated constraints, specifically using create_clock instead of create_generated_clock for the PCIe IP clocks, impacting timing and design stability.

Device affected: CertusPro-NX (LFCPNX)

Bug Number: DNG-26433

Fixed Version: R2025.2

EBR ECC parity is miscalculated in the bitstream for RAM_DP with ECC causing one_err_det/two_err_det to assert when reading any address that has not first been written in user mode.

When ECC is enabled on the DPRAM (512x32), the ECC error outputs one_err_det_o and two_err_det_o assert frequently. On hardware, the read data often does not match the written data (and this mismatch does not always coincide with the ECC error reports). In simulation, the read data always matches the write data, but one_err_det_o is asserted continuously while two_err_det_o remains 0.

Workaround: N/A.

Device affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug Number: DNG-16612, DNG-26740

Fixed Version: R2025.1

LSE may infer shift RAM as flip-flops instead of Distributed RAM/EBR on Avant

LSE may not correctly infer shift RAM structures into Distributed RAM (DRAM) or EBR. Instead, the shift RAM is implemented as a large number of flip-flops when synthesized with LSE, even though the same code infers RAM correctly with Synplify.

Workaround: N/A.

Device affected: Lattice Avant (LAV-AT)

Bug Number: DNG-20128

Fixed Version: R2024.1

ECC on EBR DPRAM may behave inconsistently between software simulation and hardware, resulting in false single-error detections.

When ECC is enabled on the DPRAM (512x32) in Jedi EBR, the ECC error outputs one_err_det_o and two_err_det_o assert frequently. On hardware, the read data often does not match the written data (and this mismatch does not always coincide with the ECC error reports). In simulation, the read data always matches the write data, but one_err_det_o is asserted continuously while two_err_det_o remains 0.

Workaround: N/A.

Device affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug Number: DNG-16612, HWII-4994

Fixed Version: R2024.2

Synplify Pro synthesis crash when using FDC-based syn_useenables

SynplifyPro reports a synthesis error after applying the FDC-based fix. In this configuration, Pipelining and Retiming is set to None. Radiant does not display any error dialog, but the SynplifyPro log shows the failure during synthesis.

Device affected: CertusPro-NX (LFCPNX)

Bug Number: DNG-23979, DNG-23499

Fixed Version: R2024.2

Synplify Pro may incorrectly infer an unsupported memory primitive "SP16K_1" during synthesis for CrossLink-NX 33U causing synthesis errors.

Workaround: Use LSE.

Devices Affected: CrossLink-NX (LIFCL-33U)

Bug Number: DNG-20643

Fixed Version: R2024.1

Radiant Programmer's "Read and Save" for XO5-100T UFM produces corrupted UFM JED files (readback values differ from on-device contents), causing programmed CFG+UFM images to fail to boot.

"Read and Save" path for XO5-100T devices where the UFM region was mis-handled during

readback, so the saved UFM JED file did not match the actual on-device UFM contents.

Workaround: N/A

Device affected: MachXO5-NX (LFMXO5)

Bug Number: DNG-26215

Fixed Version: R2025.1

Radiant Programmer may incorrectly report that the board power is not turned ON and block access to the FTUSB-2 board whenever the FTUSB-0 board is powered down. This can also occur after FTUSB device re-enumeration following a Windows reboot, even though the FTUSB 2 board remains fully powered when three HW USB 2B cables are connected.

Disconnecting a board powered via FTUSB-0 affects the accessibility of other connected boards, particularly FTUSB-2.

Workaround: N/A

Devices Affected: All devices

Bug Number: DNG-21262

Fixed Version: R2024.1

FIFO DC mixed-width configurations (different read/write data widths) produce incorrect rd_data_o values in simulation due to wrong data splitting and merging across cascaded FIFO primitives.

The FIFO DC mixed width configuration incorrectly read data in simulation.

Workaround: N/A

Device affected: CertusPro-NX (LFCPNX)

Bug Number: DNG-24678

Fixed Version: R2024.2.1

DDR3 Memory Controller IP for Certus-NX may exhibit simulation and hardware mismatches in DDR command latency due to IOLOGIC and ODDRX modeling.

Workaround: N/A

Device affected: Certus-NX (LFD2NX), Certus-NX-RT(UT24C)

Bug Number: DNG-24831

Fixed Version: R2025.1.1

Timing Analysis may not analyze paths when the DELAY (DELAYA or DELAYB) SW primitive is used as an output delay (unregistered) on Nexus IOLOGIC

When the DELAY SW primitive (DELAYA or DELAYB) is used as an output delay (unregistered) on Jedi IOLOGIC, the required timing arc may be missing in the timing data. This can cause Timing Analysis to not analyze the affected paths and can lead to post-synthesis simulation mismatches.

Workaround: The updated iologic*.tm files fix the specific issue, but additional updates may be needed for siologic*.tm and other versions like D1 and D6.

Device Affected: CrossLink-NX (LIFCL)

Bug Number: DNG-24683

Fixed Version: Future Radiant Release

Timing Analysis may not report the correct clock path delay when OSCA drives LMMI_CLK, LMMI_CLKO, or CFG_CLK on CertusPro-NX

Timing Analysis may not report the true clock path delay when OSCA drives LMMI_CLK, LMMI_CLKO, or CFG_CLK on Jedi-D1. This occurs because the OSCA to CONFIG_CLKRST_CORE timing arc is missing and the CONFIG_CLKRST_CORE to CONFIG_LMMI or SEDC path is modeled with zero delay.

Workaround: N/A

Device Affected: CertusPro-NX (LFCPNX)

Bug Number: DNG-27889

Fixed Version: Future Radiant Release

Timing Analysis may not correctly analyze ECLK tree paths due to a missing ECLK timing arc.

Timing Analysis may not correctly analyze ECLK tree paths due to a missing ECLK timing arc. This can result in inaccurate timing analysis for designs using ECLK-based paths, including paths to DQSBUF.

Devices Affected: CertusPro-NX (LFCPNX)

Bug Number: HWII-5049

Fixed Version: Future Radiant Release

Timing Analysis may not show the ODDRX4 reset timing path due to a missing timing arc, which can result in incomplete timing analysis.

Timing Analysis may not show the reset timing path for the ODDRX4 primitive. This occurs due to a missing timing arc, causing the ODDRX4 reset path to be absent from Timing Analysis and potentially resulting in incomplete timing coverage, especially when multiple ODDRX4 instances are used.

Workaround: N/A

Device Affected: CrossLink-NX (LIFCL)

Bug Number: DNG-30126

Fixed Version: Future Radiant Release

Changing the temperature setting in Timing Analyzer does not affect hold analysis results.

Changing the temperature setting in the Timing Analyzer does not affect hold analysis results. While the temperature setting impacts setup analysis, hold slacks remain unchanged and are effectively evaluated at a fixed temperature, which can lead to discrepancies when comparing Timing Analyzer results with IO timing analysis reports.

Workaround: A fix was implemented to allow temperature changes to influence timing calculations correctly, aligning IO timing reports with the Timing Analyzer.

Device Affected: Certus-NX (LFD2NX)

Bug Number: DNG-26555

Fixed Version: R2025.1

DDR clock outputs configured as differential SSTL15D may show skewed P and N waveforms instead of ideal complementary behavior.

When DDR clock outputs are configured as differential SSTL15D, the P and N output waveforms may be skewed and not fully complementary. This behavior has been observed on DDR3 IO configurations and can result in non-ideal differential clock behavior at the device pins.

Workaround: N/A

Device Affected: CertusPro-NX (LFCPNX)

Bug Number: DNG-27182

Fixed Version: R2025.2

GPLL IP may show incorrect behavior related to clock output enable control, dynamic VCO phase shifting, and lock tolerance handling in simulation.

Workaround: N/A

Device affected: CertusPro-NX (LFCPNX)

Bug number: DNG-28026

Fixed Version: R2025.2

A set_max_delay -datapath_only constraint handling bug may cause hold violations to appear in the .par report but not in Timing Analysis.

There is a mismatch between the Place & Route (PAR) report indicating hold violations and the timing analysis report showing no violations.

Workaround: N/A

Devices Affected: CertusPro-NX (LFCPNX)

Bug Number: DNG-21720

Fixed Version: R2024.1

Place & Route may terminate with an internal fatal error due to a null clock pin reference on Certus-NX devices.

Place & Route may terminate with an internal fatal error on Certus-NX designs due to code referencing a null clock pin. This issue can occur when running PAR on affected designs and prevents completion of the implementation flow.

Workaround: N/A.

Device affected: Certus-NX (LFD2NX)

Bug Number: DNG-24440

Fixed Version: R2024.1.1

When a PLL is placed in the LRC, Place & Route may use general routing instead of dedicated ECLK routing, resulting in excessive clock net delay on LFCPNX devices.

When a PLL is placed in the LRC, Place & Route may incorrectly use general routing to connect the PLL output to ECLK resources instead of dedicated routing. This can result in significantly increased clock net delays compared to designs where the PLL is placed in the LLC, even

though both locations are expected to have access to dedicated ECLK routing on LFCPNX devices.

Workaround: N/A

Devices Affected: CertusPro-NX (LFCPNX)

Bug Number: DNG-20574

Fixed Version: R2024.1

The deployment tool may generate blocks that cause issues in ping-pong boot configurations.

The deployment tool may generate blocks in a manner that causes issues in certain ping-pong boot configurations. This behavior can affect designs using ping-pong boot flows across devices and may result in unexpected boot behavior.

Workaround: Windows' plug-and-play behavior reorders USB addresses after reboots and the workaround remains to connect cables before system startup and avoid reboots after setup.

Devices Affected: All devices

Bug Number: DNG-21418

Fixed Version: R2024.1

MAP may encounter an error when running the Radiant flow on designs using a dual-rank LPDDR4 memory controller.

MAP may encounter an error when running the Radiant flow on designs that use a dual-rank LPDDR4 memory controller. This issue affects CertusPro-NX devices and can prevent successful completion of the implementation flow for affected designs.

Workaround: N/A

Devices Affected: CertusPro-NX (LFCPNX)

Bug Number: DNG-20832

Fixed Version: R2024.1

The create_generated_clock constraints defined in SDC or FDC files may be rewritten by Synplify Pro, resulting in incorrect destination clock path reporting in Timing Analysis unless it is overridden in a PDC file.

Constraints defined solely in .sdc or .fdc files cause incorrect destination clock paths and timing failures during synthesis and place & route.

Workaround: Define the create_generated_clock constraint in the .pdc or let the Radiant timer auto-generate the constraint.

Devices Affected: All devices

Bug Number: DNG-20228

Fixed Version: R2024.1

RAM_DP_True may output zeroes and fail to retain data at address 0x800 during certain transactions.

RAM_DP_True may output zeroes and fail to retain data at address 0x800 during certain transactions. This issue affects Lattice Avant devices and can result in incorrect memory behavior under specific access patterns.

Workaround: With output registers enabled, assert clk_en_x_i for 2 clock cycles whenever you pipeline the output data so the RAM_DP_True output at address 0x800 correctly retains its value during the transaction.

Devices Affected: Lattice Avant (LAV-AT)

Bug Number: DNG-20532

Fixed Version: R2024.1

Unexpanded interface port error during synthesis with Synplify Pro for some designs using the System Verilog interface construct.

Workaround: N/A

Devices Affected: CrossLink-NX (LIFCL)

Bug Number: DNG-19872

Fixed Version: R2024.1

Known Issues for Radiant 2023.2.1

The following are known issues for Radiant Software 2023.2.1.

When simulating GDDR 7:1 with RX configuration, and Bandwidth is around 935 Mbps to 945 Mbps, there may be a mismatch in the RTL, Post-Synthesis, and Post-PAR simulation due to a change in the PLL simulation model.

Workaround: On the customer testbench, tb_top.v, where pll_rstn_i signal is asserted and

deasserted, increase the pll_rstn_i time. This can be done by increasing the number inside the parentheses after the word “repeat.” The suggested number is 8 or 10 or any greater number.

Device affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink- NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug Number: DNG-20829

LSE mishandles the "syn_black_box=1" attribute on IP generated instance ram_dp_inst_inst.

Workaround: Remove "syn_black_box=1" from the source design to complete synthesis.

Device affected: All Devices

Bug Number: DNG-20764

The value of the 32-bit hardware IDCODE is 0 when running RTL simulation.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CertusPro-NX (LFCPNX), CrossLink-NX (LIFCL-33, LIFCL 33U), MachXO5-NX (LFMXO5)

Bug number: DNG-20754

ModelSim program error occurs when running the RTL simulation of CONFIG_LMMIB.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: MachXO5-NX (LFMXO5-25)

Bug number: DNG-20755

CONFIG_LMMIE RTL simulation error occurs, LMMIRDATA port prompts incorrect data.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: MachXO5-NX (LFMXO5-100T)

Bug number: DNG-20666

Reveal trigger feature error occurs for JTAG merge case.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20610

An error occurs when using PLL CLKOS4 RCLK due to PLL and CDC registers placement issue.

Workaround: Change from CLKOS4 to CLKOS3 to use GCLK instead of RCLK.

Device Affected: Lattice Avant (LAV-AT)

Bug Number: DNG-20599

Synplify reports an error message for JTAG merge in Reveal Analyzer.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20598

CONFIG_LMMI RTL simulation error occurs and data missing in output ports.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20543

Incorrect calculation for LFM airflow when adjusting the Thermal Profile in Power Calculator.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20485

SEI Editor issues related with different devices.

1. Nexus devices (LIFCL-17K, LFD2NX-17K, and LFMXO5-25K) cannot support SEI 2-bit with Unused strategy for combinations such as EBR-EBR or DSP-DSP.
2. The requirement for SEI 2-bit is that both error bits should be in the same data frame. The data frame corresponds to the FPGA column with reference to the "array" architecture.
3. In Nexus architecture, any device with a density less than 30K has only 1 EBR or 1 DSP per column. Due to this limitation, it cannot support multiple error injection on an EBR or DSP site for these densities.

4. However, those device densities can support SEI 2-bit Random strategy combinations and SEI 2-bit PFU-PFU combination with Unused strategy.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-19715

IBIS reports I/O models of some sysCONFIG pins even if they are used as GPIO.

Workaround: Remove duplicated pins in IBIS file.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19646

AON Case with Cadence Xcelium does not correctly recognize the number of ports on a user defined primitive.

Workaround: Use other simulators for the simulation, such as QuestaSim, VCS.

Devices affected: CrossLink-NX (LIFCL-33U)

Bug number: DNG-19623

Avant input I/O cannot be set as MIPI_DPHY type.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19199

When using LSE, post-synthesis engine may fail with the following error: “ERROR <1025017> - Not user declared module (VERIFIC_AND).”

This error occurs when the MOD operator is used.

Workaround: Replace the MOD operator to avoid this issue.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-16713

The PHASEDIR function of PLL does not work, the phase shift of

CLKOS is still delayed when PHASEDIR = 1.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-16440

When using ModelSim to run Post-Route Gate-Level or Post-Route Gate-Level+Timing simulation, Modelsim may crash if you use a large design file, with error message “Fatal: (vsim-4) ****** Memory allocation failure.”

Workaround: Use QuestaSim 64-bit version.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-14945

When simulating Cordic IP using ModelSim, you may encounter an error during simulation.

Workaround: In OEM ModelSim, use the “vsim -voptargs=+acc -L work -L pmi_work -L ovi_lavat tb_top -suppress 8607” command to finish the simulation.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-14888

Reveal Power-on Reset (POR) Debug function does not work when using LSE with only one Trigger Unit (TU).

Workaround: Add another Trigger Unit that can be unrelated to POR Debug.

Devices affected: All devices except iCE40 UltraPlus (iCE40UP)

Bug number: DNG-13901

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Workaround: Use Modelsim simulation tool.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

When simulating Generic DDR, there may be a mismatch in the RTL and post-route simulation. Silicon is not affected.

Workaround: For Nexus devices, intrinsic delay similar to the delay value on the vo.vo file needs to be added to the IP testbench.

For Avant devices, overwrite the delay parameter values of the primitives used on the GDDR instance with the same value from the generated RTL on the generated post-PAR netlist. This should only be done for simulation purposes.

Devices affected: All devices except iCE40 UltraPlus (iCE40UP)

Bug number: DNG-9639, DNG-18794

MAP incorrectly reports the number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

Workaround: Issue relates to DNG-10587 and MAP has been updated using the new API for DPHY.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297